EXHIBIT 1

FAIRCHILD SEMICONDUCTOR®

April 2007

FSQ0170RNA, FSQ0270RNA, FSQ0370RNA
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged 700V SenseFET
- Consumes only 0.8W at 230 V_{AC} & 0.5W Load with Burst-Mode Operation
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft-Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over-Voltage Protection (OVP), Overload Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under-Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player, Printer, Facsimile & Scanner
- Adapter for Camcorder

Related Application Notes

- *AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)*
- *AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)*
- *AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147: Design Guidelines for RCD Snubber of Flyback*
- *AN-4148: Audible Noise Reduction Techniques for FPS™ Applications*

Description

The FSQ0170RNA, FSQ0270RNA, FSQ0370RNA consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V Sense FET. It is specifically designed for high-performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include: a fixed-frequency generating oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSQ0170RNA, FSQ0270RNA, FSQ0370RNA reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, as in PC auxiliary power supplies.

8-DIP

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$ (MAX.)
FSQ0170RNA	8DIP	Q0170R	700V	100kHz	11Ω
FSQ0270RNA	8DIP	Q0270R	700V	100kHz	7.2Ω
FSQ0370RNA	8DIP	Q0370R	700V	100kHz	4.75Ω

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Application Diagram

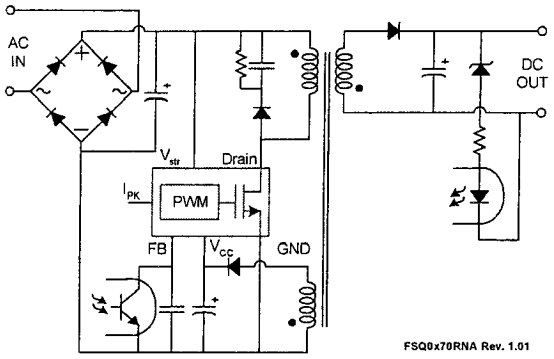


Figure 1. Typical Flyback Application

Output Power Table[1]

Product	230V$_{AC}$ ±15%[2]		85–265V$_{AC}$	
	Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]
FSQ0170RNA	14W	20W	9W	13W
FSQ0270RNA	17W	24W	11W	16W
FSQ0370RNA	20W	27W	13W	19W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at 50°C ambient.

Internal Block Diagram

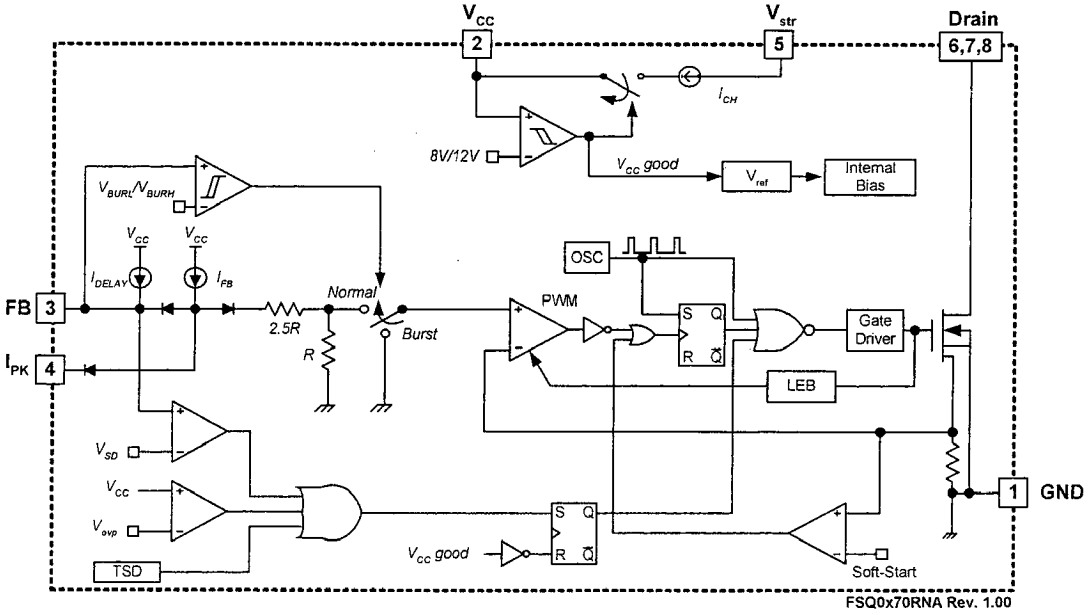


Figure 2. Internal Block Diagram

Pin Configuration

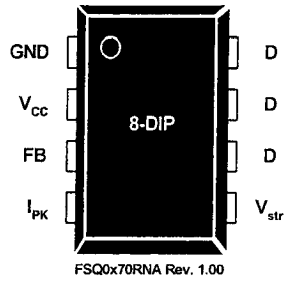


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground.** SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	**Power Supply.** Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{str}) via an internal switch during start-up, see Figure 2. It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	FB	**Feedback.** The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a time delay while charging external capacitor C_{FB} from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	I_{PK}	**Peak Current Limit.** This pin adjusts the peak current limit of the SenseFET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to V_{CC} or left floating, the typical peak current limit is 0.8A (FSQ0170RNA), 0.9A (FSQ0270RNA), or 1.1A (FSQ0370RNA).
5	V_{str}	**Start-up.** This pin connects to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once the V_{CC} reaches 12V, the internal switch is opened.
6	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.
7	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.
8	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. T_A = 25°C, unless otherwise specified.

Symbol	Characteristic		Value	Unit
V_{DRAIN}	Drain Pin Voltage		700	V
V_{STR}	Vstr Pin Voltage		700	V
I_{DM}	Drain Current Pulsed[5]	FSQ0170RNA	4	A
		FSQ0270RNA	8	
		FSQ0370RNA	12	
E_{AS}	Single Pulsed Avalanche Energy[6]	FSQ0170RNA	50	mJ
		FSQ0270RNA	140	
		FSQ0370RNA	230	
V_{CC}	Supply Voltage		20	V
V_{FB}	Feedback Voltage Range		-0.3 to V_{CC}	V
P_D	Total Power Dissipation		1.5	W
T_J	Operating Junction Temperature		Internally limited	°C
T_A	Operating Ambient Temperature		-25 to +85	°C
T_{STG}	Storage Temperature		-55 to +150	°C

Notes:

5. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
6. L = 51mH, starting T_J = 25°C.

Thermal Impedance

T_A = 25°C, unless otherwise specified. All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance[7]	80	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance[8]	20	°C/W
θ_{JT}	Junction-to-Top Thermal Resistance[9]	35	°C/W

Notes:

7. Free standing with no heatsink; without copper clad.
   (Measurement Condition - Just before junction temperature T_J enters into OTP.)
8. Measured on the DRAIN pin close to plastic interface.
9. Measured on the PKG top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SenseFET Section[10]							
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 700V, V_{GS} = 0V			50	μA
			V_{DS} = 560V, V_{GS} = 0V, T_C = 125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[11]	FSQ0170RNA	V_{GS} = 10V, I_D = 0.5A		8.8	11	Ω
		FSQ0270RNA			6.0	7.2	
		FSQ0370RNA			4.0	4.75	
C_{ISS}	Input Capacitance	FSQ0170RNA	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		250		pF
		FSQ0270RNA			550		
		FSQ0370RNA			315		
C_{OSS}	Output Capacitance	FSQ0170RNA			25		
		FSQ0270RNA			38		
		FSQ0370RNA			47		
C_{RSS}	Reverse Transfer Capacitance	FSQ0170RNA			10		
		FSQ0270RNA			17		
		FSQ0370RNA			9		
$t_{d(on)}$	Turn-On Delay Time	FSQ0170RNA	V_{DS} = 350V, I_D = 1.0A		12		ns
		FSQ0270RNA			20		
		FSQ0370RNA			11.2		
t_r	Rise Time	FSQ0170RNA			4		
		FSQ0270RNA			15		
		FSQ0370RNA			34		
$t_{d(off)}$	Turn-Off Delay Time	FSQ0170RNA			30		
		FSQ0270RNA			55		
		FSQ0370RNA			28.2		
t_f	Fall Time	FSQ0170RNA			10		
		FSQ0270RNA			25		
		FSQ0370RNA			32		
Control Section							
f_{OSC}	Switching Frequency			92	100	108	KHz
Δf_{OSC}	Switching Frequency Variation[10]		-25°C ≤ T_A ≤ 85°C		±5	±10	%
D_{MAX}	Maximum Duty Cycle		Measured at 0.1 x V_{DS}	55	60	65	%
D_{MIN}	Minimum Duty Cycle			0	0	0	%
V_{START}	UVLO Threshold Voltage		V_{FB} = GND	11	12	13	V
V_{STOP}			V_{FB} = GND	7	8	9	
I_{FB}	Feedback Source Current		V_{FB} = GND	0.7	0.9	1.1	mA
$t_{S/S}$	Internal Soft-Start Time[10]		V_{FB} = 4V		10		ms

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Burst-Mode Section							
V_{BURH}	Burst-Mode Voltage		T_J = 25°C	0.5	0.6	0.7	V
V_{BURL}				0.3	0.4	0.5	V
$V_{BUR(HYS)}$				100	200	300	mV
Protection Section							
I_{LIM}	Peak Current Limit	FSQ0170RNA	di/dt = 170mA/µs	0.70	0.80	0.90	A
		FSQ0270RNA	di/dt = 200mA/µs	0.79	0.90	1.01	
		FSQ0370RNA	di/dt = 240mA/µs	0.97	1.10	1.23	
t_{CLD}	Current Limit Delay Time(10)				500		ns
T_{SD}	Thermal Shutdown Temperature(10)			125	140		°C
V_{SD}	Shutdown Feedback Voltage			5.5	6.0	6.5	V
V_{OVP}	Over-Voltage Protection			18	19		V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 4V	3.5	5.0	6.5	µA
t_{LEB}	Leading Edge Blanking Time(10)			200			ns
Total Device Section							
I_{OP}	Operating Supply Current (control part only)		V_{CC} = 14V	1	3	5	mA
I_{CH}	Start-Up Charging Current		V_{CC} = 0V	0.70	0.85	1.00	mA
V_{STR}	V_{str} Supply Voltage		V_{CC} = 0V		24		V

Notes:

10. These parameters, although guaranteed, are not 100% tested in production.
11. Pulse test: Pulse width ≤ 300µs, duty ≤ 2%.

Typical Performance Characteristics (Control Part)

These characteristic graphs are normalized at T_A= 25°C.

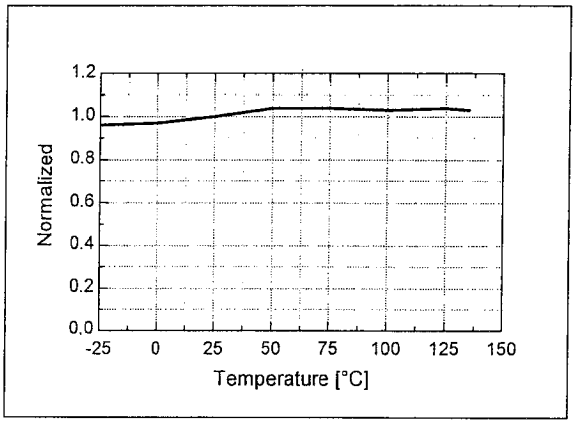


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

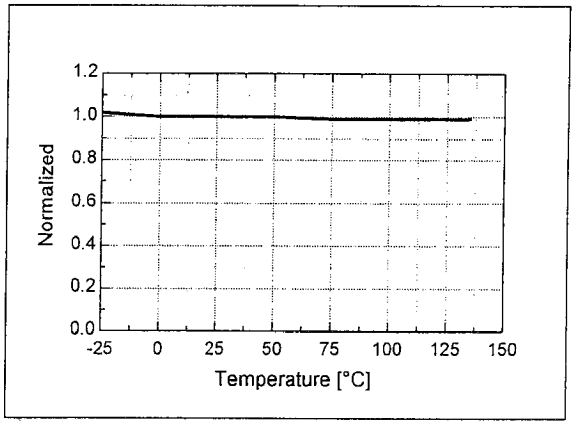


Figure 5. Over-Voltage Protection (V_{OVP}) vs. T_A

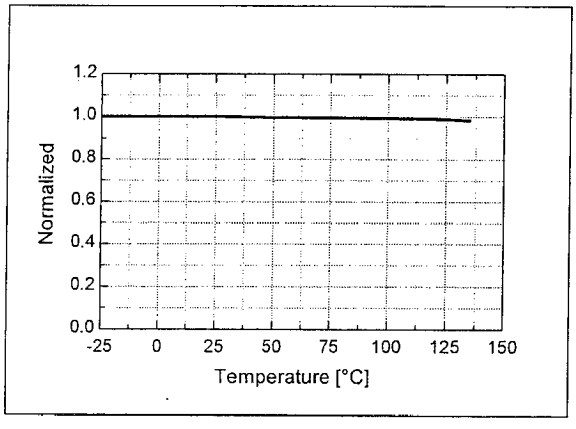


Figure 6. Maximum Duty Cycle (D_{MAX}) vs. T_A

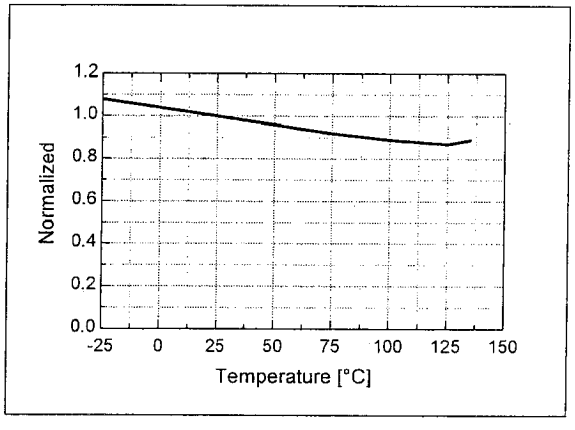


Figure 7. Operating Supply Current (I_{OP}) vs. T_A

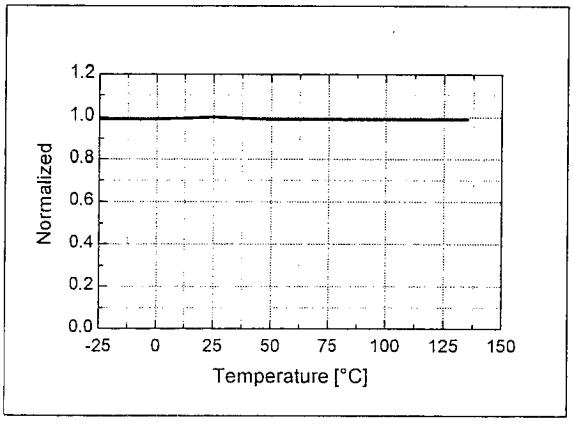


Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

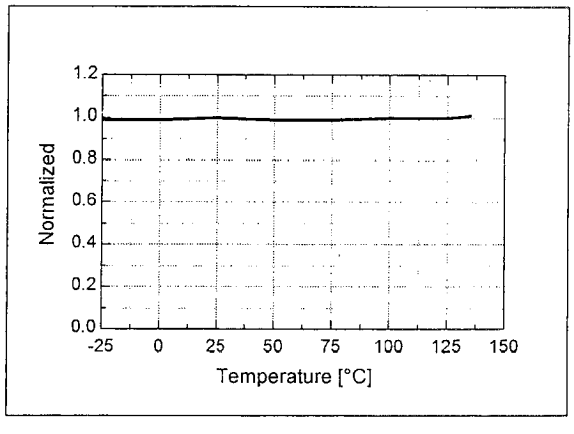


Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

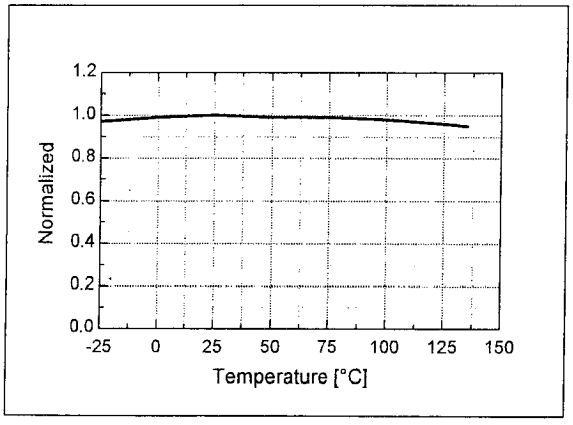


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

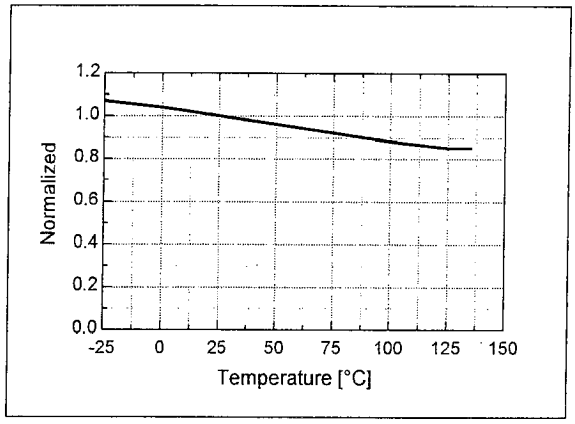


Figure 11. Start-Up Charging Current (I_{CH}) vs. T_A

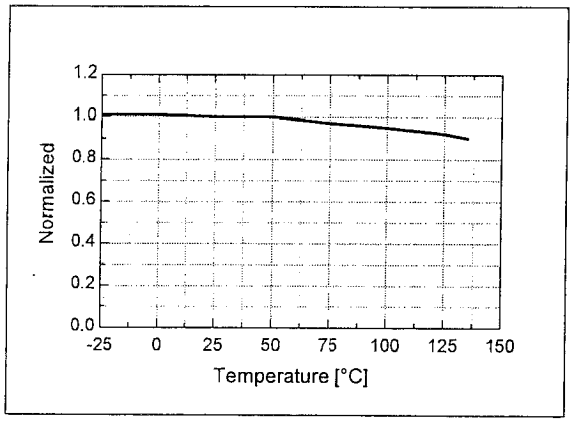


Figure 12. Peak Current Limit (I_{LIM}) vs. T_A

Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™), the V_{str} pin required an external resistor to the DC input voltage line. In this generation, the startup resistor is replaced by an internal high-voltage current source and a switch that shuts off 10ms after the supply voltage, V_{CC}, goes above 12V. The source turns back on if V_{CC} drops below 8V.

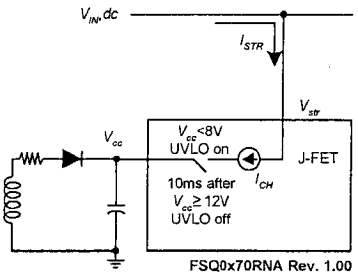


Figure 13. High-Voltage Current Source

2. Feedback Control: The 700V FPS series employs current-mode control, as shown in Figure 14. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor of SenseFET, plus an offset voltage, makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down and thereby reduces the duty cycle. This typically happens when the input voltage increases or the output load decreases.

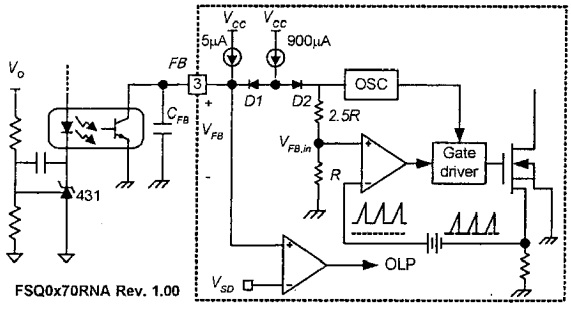


Figure 14. Pulse Width Modulation Circuit

3. Leading Edge Blanking (LEB): When the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{sense} resistor leads to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FPS employs a Leading Edge Blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits: The FPS has several protective functions, such as Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), and Thermal Shutdown (TSD). Because these protection circuits are fully integrated in the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage, V_{STOP} (typically 8V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{str} pin. When V_{CC} reaches the UVLO start voltage, V_{START} (typically 12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the OLP circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or a true overload situation. In conjunction with the I_{PK} current limit pin (if used), the current mode feedback path limits the current in the SenseFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_O) decreases below nominal voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to slowly charge C_{FB} up to V_{CC}. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated, as shown in Figure 15. The shutdown delay time is the time required to charge C_{FB} from 3V to 6V with 5μA current source.

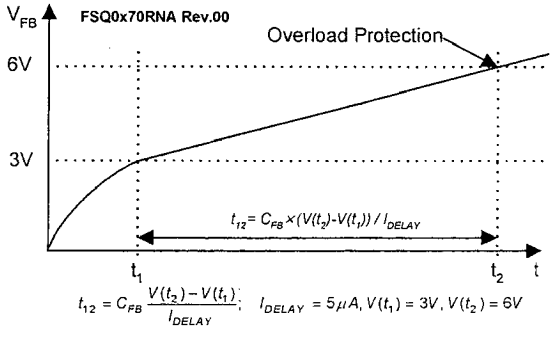


Figure 15. Overload Protection (OLP)

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control

IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Over-Voltage Protection (OVP): In the event of a malfunction in the secondary-side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (see Figure 14). V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an Over-Voltage Protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, the OVP circuit is activated, resulting in termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 19V.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the SenseFET current after start-up, as shown in Figure 16. The typical soft-start time is 10ms, where progressive increments of the SenseFET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

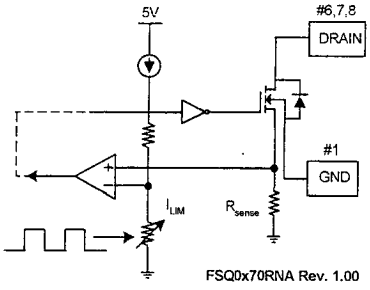


Figure 16. Soft-Start Function

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. Feedback voltage decreases as the load decreases, as shown in Figure 17, and the device automatically enters burst-mode when the feedback voltage drops below V_{BURH} (typically 600mV). Switching continues until the feedback voltage drops below V_{BURL} (typically 400mV). At this point, switching stops and the output voltage starts to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process is repeated. Burst-mode operation alternately enables and disables switching of the SenseFET and reduces switching loss in standby mode.

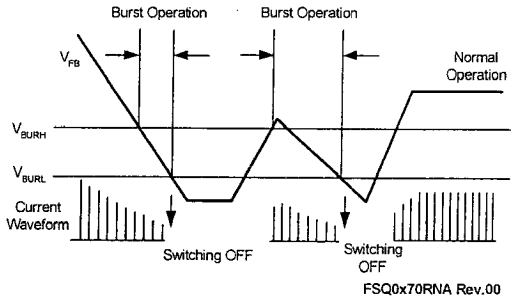


Figure 17. Burst Operation Function

7. Adjusting Peak Current Limit: As shown in Figure 18, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

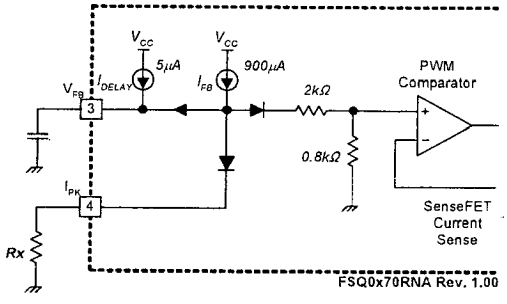


Figure 18. Peak Current Limit Adjustment

For example, FSQ0270RNA has a typical SenseFET peak current limit (I_{LIM}) of 0.9A. I_{LIM} can be adjusted to 0.6A by inserting Rx between the I_{PK} pin and the ground. The value of the Rx can be estimated by the following equations:

0.9A: 0.6A = 2.8kΩ : XkΩ,

$X = Rx \parallel 2.8k\Omega$

where X represents the resistance of the parallel network.

Application Information

Methods of Reducing Audible Noise

Switching-mode power converters have electronic and magnetic components, which generate audible noise when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise, depending on the load condition. The following sections discuss methods to reduce noise.

Glue or Varnish

The most common method of reducing noise involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. Glue or varnish can also can crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. Another possibility is to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of the 2~4kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, the noise sounds louder although the noise intensity level is identical (see Figure 19).

When the FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst mode operation lies in the range of 2~4kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D); and feedback capacitor (C_B), and decrease a feedback gain resistor (R_F), as shown in Figure 20.

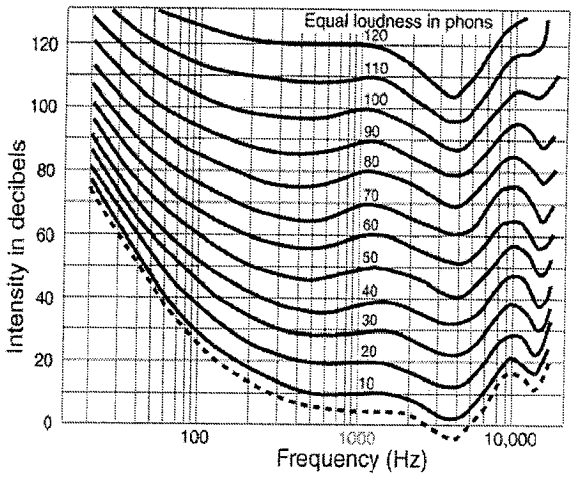


Figure 19. Equal Loudness Curves

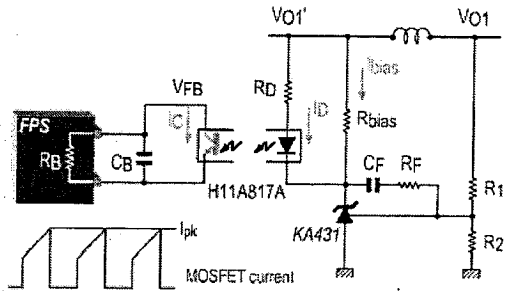


Figure 20. Typical Feedback Network of FPS

Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

Typical Application Circuit

Application	Output power	Input Voltage	Output Voltage (Max. Current)
PC Auxiliary Power Supply (Using FSQ0270RNA)	15W	Universal input (85-265 V_{AC})	5V (3A)

Features

- High efficiency (> 78% at 115 V_{AC} and 230 V_{AC} input)
- Low standby mode power consumption (< 0.8W at 230 V_{AC} input and 0.5W load)
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)
- Line UVLO function can be achieved using external component

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C8 of 47nF. If faster/slower triggering of OLP is required, C8 can be changed to a smaller/larger value (e.g. 100nF for about 60ms).
- ZP1, DL1, RL1, RL2, RL3, RL4, RL5, RL7, QL1, QL2, and CL9 build a Line Under-Voltage Lockout block (UVLO). The Zener voltage of ZP1 determines the input voltage that makes FPS turn on. RL5 and DL1 provide a reference voltage from V_{CC}. If the input voltage divided by RL1, RL2, and RL4 is lower than the Zener voltage of DL1, QL1 and QL2 turn on and pull down V_{FB} to ground.
- An evaluation board and corresponding test report can be provided.

1. Schematic

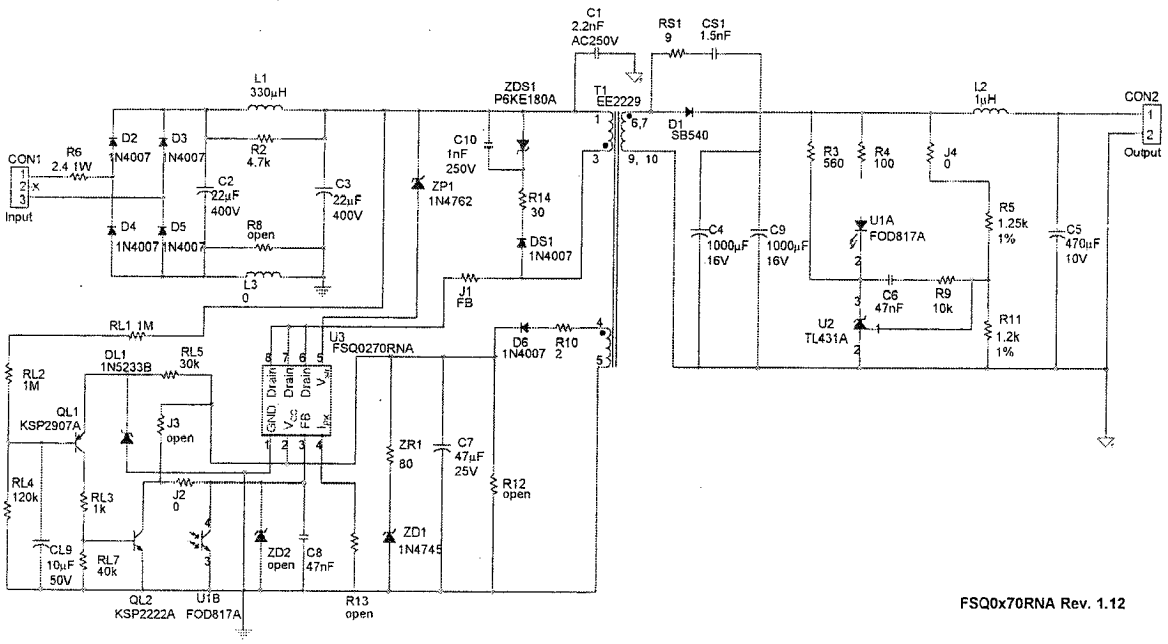


Figure 21. Demo Circuit

2. Transformer

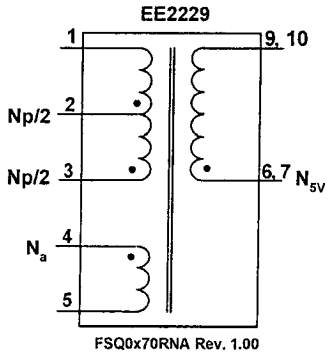


Figure 22. Transformer Schematic Diagram

3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 1 Layers				
N_a	4 → 5	0.25φ × 2	22	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{5V}	6, 7 → 9, 10	0.65φ × 2	8	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				

4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1–3	1.20mH ± 5%	100kHz, 1V
Leakage	1–3	< 30μH Max	Short all other pins

5. Core & Bobbin

- Core: EE2229 (Material: PL-7, Ae = 35.7 mm^2)
- Bobbin: BE2229

6. Demo Circuit Part List

Part Number	Value	Quantity	Description (Manufacturer)
C6, C8	47nF	2	Ceramic Capacitor
C1	2.2nF (1KV)	1	AC Ceramic Capacitor(X1 & Y1)
C10	1nF (200V)	1	Mylar Capacitor
CS1	1.5nF (50V)	1	Ceramic Capacitor
C2, C3	22μF (400V)	2	Low Impedance Electrolytic Capacitor KMX series
C4, C9	1000μF (16V)	2	Low ESR Electrolytic Capacitor NXC series
C5	470μF (10V)	1	Low ESR Electrolytic Capacitor NXC series
C7	47μF (25V)	1	General Electrolytic Capacitor
CL9	10μF (50V)	1	General Electrolytic Capacitor
L1	330μH	1	Inductor
L2	1μH	1	Inductor
R6	2.4 (1W)	1	Fusible Resistor
J1, J2, J4, L3	0	4	Jumper
R2	4.7kΩ	1	Resistor
R3	560Ω	1	Resistor
R4	100Ω	1	Resistor
R5	1.25kΩ	1	Resistor
R11	1.2kΩ	1	Resistor
R9	10kΩ	1	Resistor
R10	2Ω	1	Resistor
R14	30Ω	1	Resistor
RL3	1kΩ	1	Resistor
RL1, RL2	1MΩ	2	Resistor
RL4	120kΩ	1	Resistor
RL5	30kΩ	1	Resistor
RL7	40kΩ	1	Resistor
RS1	9Ω	1	Resistor
ZR1	80Ω	1	Resistor
U1	FOD817A	1	IC (Fairchild Semiconductor)
U2	TL431	1	IC (Fairchild Semiconductor)
U3	FSQ0270RNA	1	IC (Fairchild Semiconductor)
QL1	2N2907	1	IC (Fairchild Semiconductor)
QL2	2N2222	1	IC (Fairchild Semiconductor)
D2, D3, D4, D5, D6, DS1	1N4007	6	Diode (Fairchild Semiconductor)
D1	SB540	1	Schottky Diode (Fairchild Semiconductor)
ZD1	1N4745	1	Zener Diode (Fairchild Semiconductor)
DL1	1N5233	1	Zener Diode (Fairchild Semiconductor)
ZP1	82V (1W)	1	Zener Diode (Fairchild Semiconductor)
ZDS1	P6KE180A	1	TVS (Fairchild Semiconductor)

7. Layout

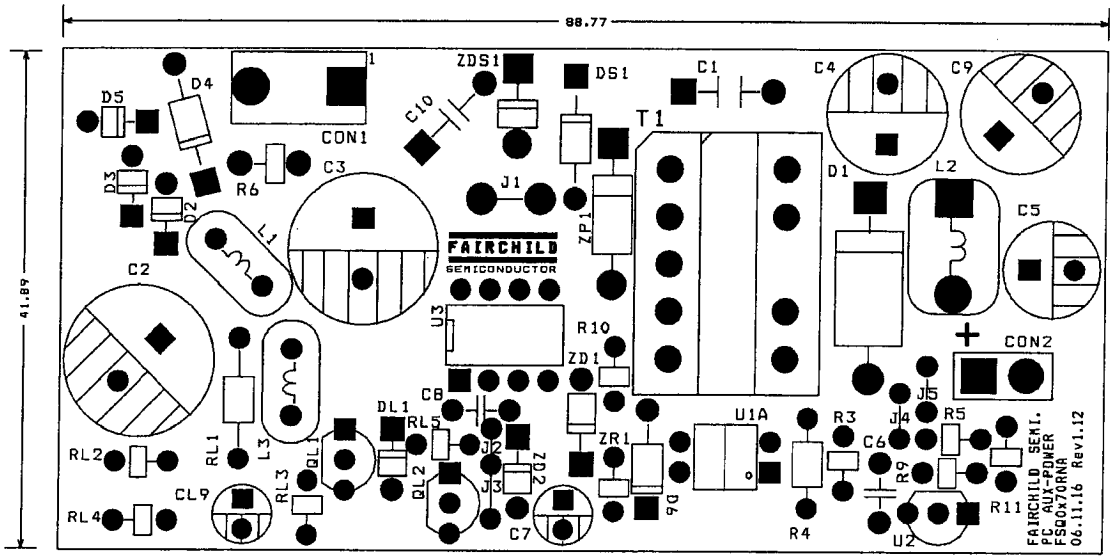


Figure 23. Top Image of PCB

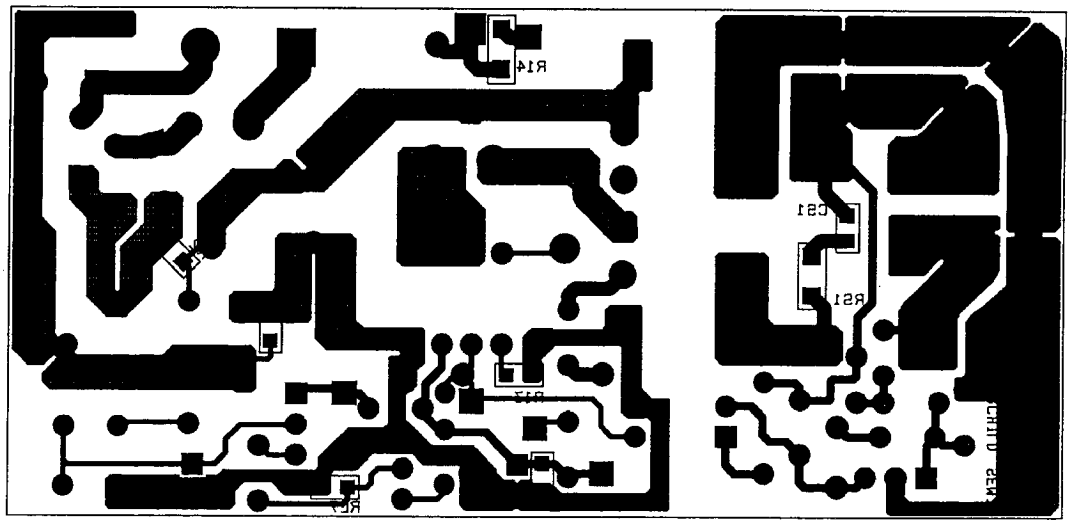
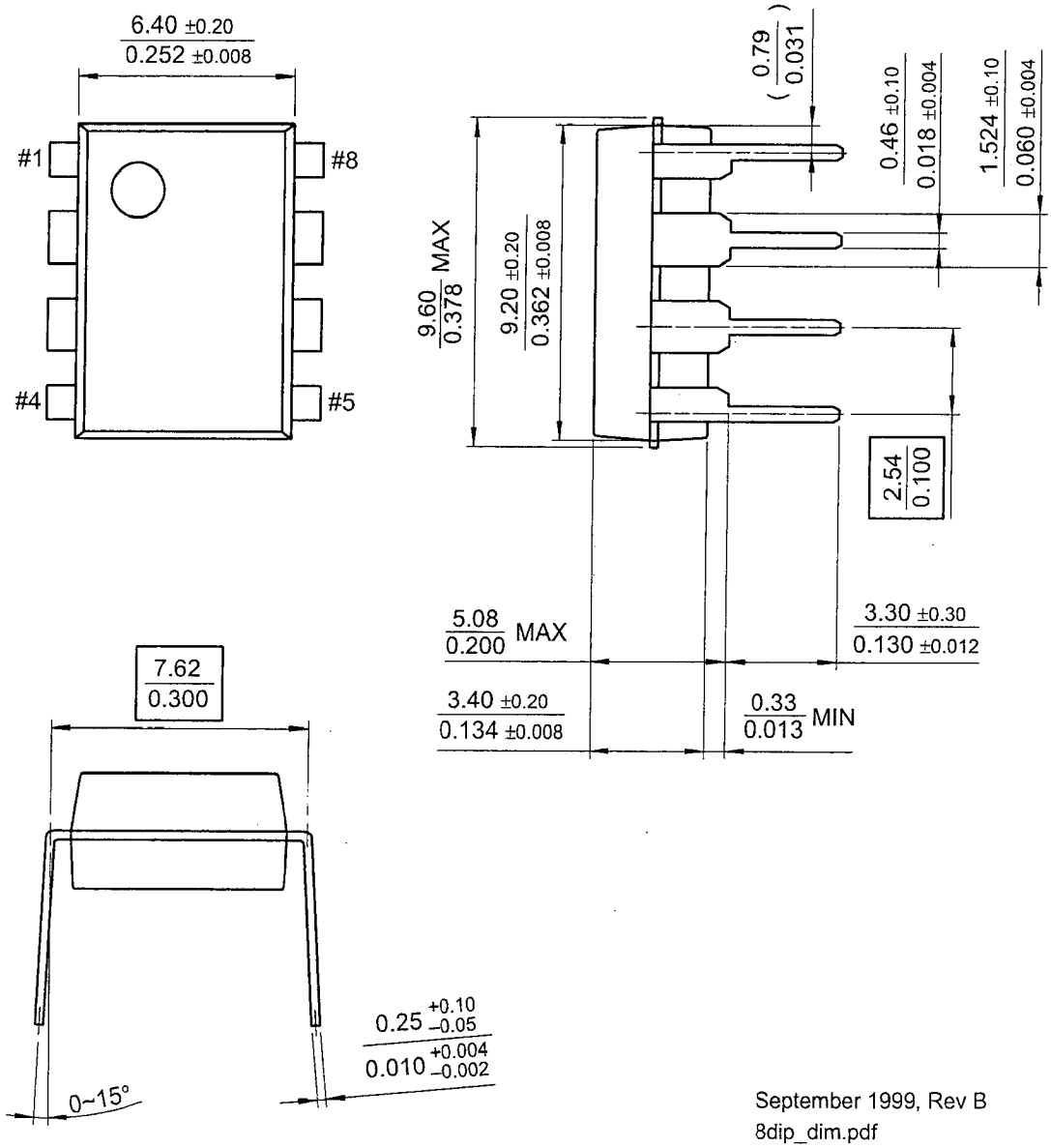


Figure 24. Bottom Image of PCB

Package Dimensions

8-DIP

Dimensions are in millimeters unless otherwise noted.



September 1999, Rev B
8dip_dim.pdf

Figure 25. 8-Lead Dual In-Line Package (DIP)

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OCX™
OCXPro™
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POP™
Power220®
Power247®
PowerEdge™
PowerSaver™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
The Power Franchise®
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I26

EXHIBIT 2

March 2006

FAIRCHILD SEMICONDUCTOR®

FSDH0170RNB/FSDH0270RNB/FSDH0370RNB
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged 700V Sense FET
- Consumes only 0.8W at 230 VAC & 0.5W load with Burst-Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over Voltage Protection (OVP), Over Load Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player
- SMPS for Printer, Facsimile & Scanner
- Adapter for Camcorder

Related Application Notes

- AN-4137, AN-4141, AN-4147 (Flyback)
- AN-4134 (Forward)

Description

The FSDH0170RNB/FSDH0270RNB/FSDH0370RNB consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche rugged 700V Sense FET. It is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include : a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDH0170RNB/FSDH0270RNB/FSDH0370RNB reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, as in PC auxiliary power supplies.

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$ (MAX.)
FSDH0170RNB	8DIP	DH0170R	700V	100KHz	11Ω
FSDH0270RNB	8DIP	DH0270R	700V	100KHz	7.2Ω
FSDH0370RNB	8DIP	DH0370R	700V	100KHz	4.75Ω

Typical Circuit

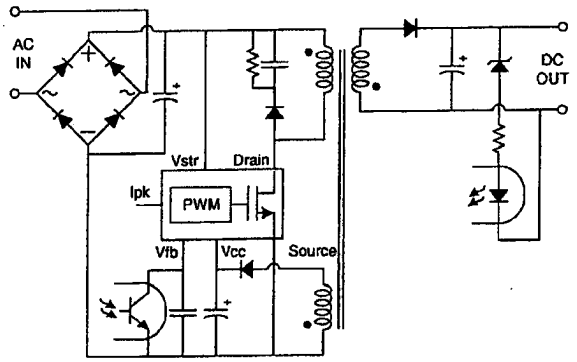


Figure 1. Typical Flyback Application

Output Power Table[4]

Product	230VAC ±15%[3]		85–265VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
FSDH0170RNB	14W	20W	9W	13W
FSDH0270RNB	17W	24W	11W	16W
FSDH0370RNB	20W	27W	13W	19W

Notes:
1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.
4. The maximum output power can be limited by junction temperature.

Internal Block Diagram

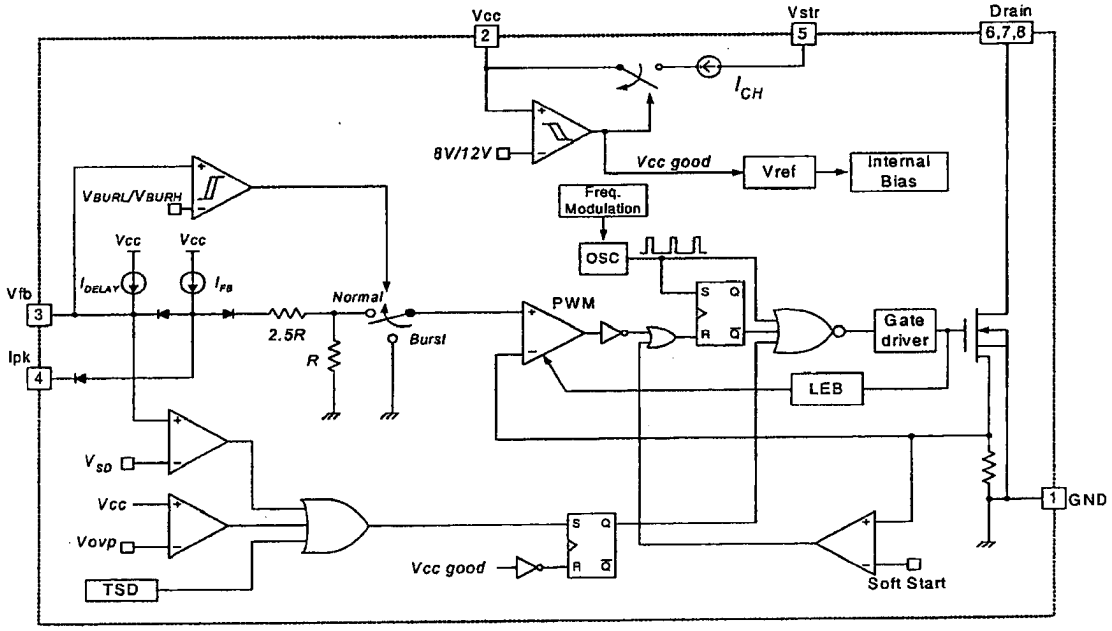


Figure 2. Functional Block Diagram of FSDH0170RNB/FSDH0270RNB/FSDH0370RNB

Pin Configuration

8DIP

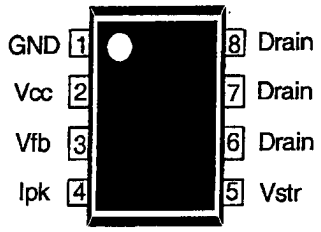


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram Section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	Ipk	This pin adjusts the peak current limit of the Sense FET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit will be 0.8A (FSDH0170RNB), 0.9A (FSDH0270RNB), or 1.1A (FSDH0370RNB).
5	Vstr	This pin connects to the rectified AC line voltage source. At start-up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DRAIN}	Drain Pin Voltage		700	V
V_{STR}	Vstr Pin Voltage		700	V
I_{DM}	Drain Current Pulsed[5]	FSDH0170RNB	4	A
		FSDH0270RNB	8	A
		FSDH0370RNB	12	A
E_{AS}	Single Pulsed Avalanche Energy[6]	FSDH0170RNB	50	mJ
		FSDH0270RNB	140	mJ
		FSDH0370RNB	230	mJ
V_{CC}	Supply Voltage		20	V
V_{FB}	Feedback Voltage Range		-0.3 to V_{CC}	V
P_D	Total Power Dissipation		1.5	W
T_J	Operating Junction Temperature		Internally limited	°C
T_A	Operating Ambient Temperature		-25 to +85	°C
T_{STG}	Storage Temperature		-55 to +150	°C

Thermal Impedance

(T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Value	Unit
8 DIP			
θ_{JA}	Junction-to-Ambient Thermal[7]	80	°C/W
θ_{JC}	Junction-to-Case Thermal[8]	20	°C/W
Ψ_{JT}	Junction-to-Top Thermal[9]	35	°C/W

All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Notes:

5. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
6. L = 51mH, starting Tj = 25°C.
7. Free standing with no heatsink; Without copper clad.
8. Measured on the DRAIN pin close to plastic interface.
9. Measured on the PKG top surface.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Sense FET Section[11]							
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 700V, V_{GS} = 0V	–	–	50	μA
			V_{DS} = 560V, V_{GS} = 0V, T_C = 125°C	–	–	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[10]	FSDH0170RNB	V_{GS} = 10V, I_D = 0.5A	–	8.8	11	Ω
		FSDH0270RNB		–	6.0	7.2	
		FSDH0370RNB		–	4.0	4.75	
C_{ISS}	Input Capacitance	FSDH0170RNB	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	250	–	pF
		FSDH0270RNB		–	550	–	
		FSDH0370RNB		–	315	–	
C_{OSS}	Output Capacitance	FSDH0170RNB		–	25	–	
		FSDH0270RNB		–	38	–	
		FSDH0370RNB		–	47	–	
C_{RSS}	Reverse Transfer Capacitance	FSDH0170RNB		–	10	–	
		FSDH0270RNB		–	17	–	
		FSDH0370RNB		–	9	–	
$t_{d(on)}$	Turn-On Delay Time	FSDH0170RNB	V_{DS} = 350V, I_D = 1.0A	–	12	–	ns
		FSDH0270RNB		–	20	–	
		FSDH0370RNB		–	11.2	–	
t_r	Rise Time	FSDH0170RNB		–	4	–	
		FSDH0270RNB		–	15	–	
		FSDH0370RNB		–	34	–	
$t_{d(off)}$	Turn-Off Delay Time	FSDH0170RNB		–	30	–	
		FSDH0270RNB		–	55	–	
		FSDH0370RNB		–	28.2	–	
t_f	Fall Time	FSDH0170RNB		–	10	–	
		FSDH0270RNB		–	25	–	
		FSDH0370RNB		–	32	–	
Control Section							
f_{OSC}	Switching Frequency			92	100	108	KHz
Δf_{MOD}	Switching Frequency Modulation			±2	±3	±4	KHz
Δf_{OSC}	Switching Frequency Variation[11]		-25°C ≤ T_A ≤ 85°C	–	±5	±10	%
D_{MAX}	Maximum Duty Cycle		Measured @0.1 x Vds	62	67	72	%
D_{MIN}	Minimum Duty Cycle			0	0	0	%
V_{START}	UVLO Threshold Voltage		V_{FB} = GND	11	12	13	V
V_{STOP}			V_{FB} = GND	7	8	9	
I_{FB}	Feedback Source Current		V_{FB} = GND	0.7	0.9	1.1	mA
$t_{S/S}$	Internal Soft Start Time[11]		V_{FB} = 4V	–	10	–	ms

Electrical Characteristics (Continued)

(T_A = 25°C unless otherwise specified)

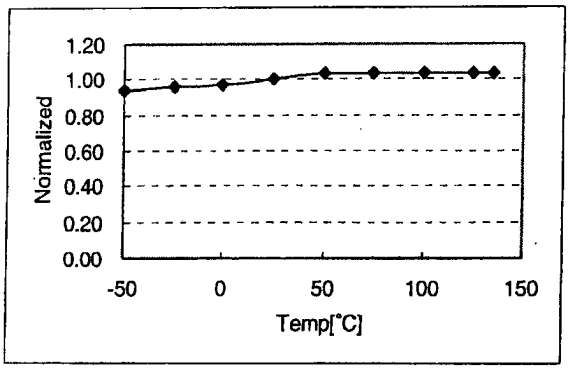
Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Burst Mode Section							
V_{BURH}	Burst Mode Voltage		Tj = 25°C	0.5	0.6	0.7	V
V_{BURL}				0.3	0.4	0.5	V
$V_{BUR(HYS)}$				100	200	300	mV
Protection Section							
I_{LIM}	Peak Current Limit	FSDH0170RNB	di/dt = 170mA/µs	0.70	0.80	0.90	A
		FSDH0270RNB	di/dt = 200mA/µs	0.79	0.90	1.01	
		FSDH0370RNB	di/dt = 240mA/µs	0.97	1.10	1.23	
t_{CLD}	Current Limit Delay Time[11]			–	500	–	ns
T_{SD}	Thermal Shutdown Temperature[11]			125	140	–	°C
V_{SD}	Shutdown Feedback Voltage			5.5	6.0	6.5	V
V_{OVP}	Over Voltage Protection			18	19	–	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 4V	3.5	5.0	6.5	µA
t_{LEB}	Leading Edge Blanking Time[11]			200	–	–	ns
Total Device Section							
I_{OP}	Operating Supply Current (control part only)		V_{CC} = 14V	1	3	5	mA
I_{CH}	Start-Up Charging Current		V_{CC} = 0V	0.7	0.85	1.0	mA
V_{STR}	Vstr Supply Voltage		V_{CC} = 0V	–	24	–	V

Notes:

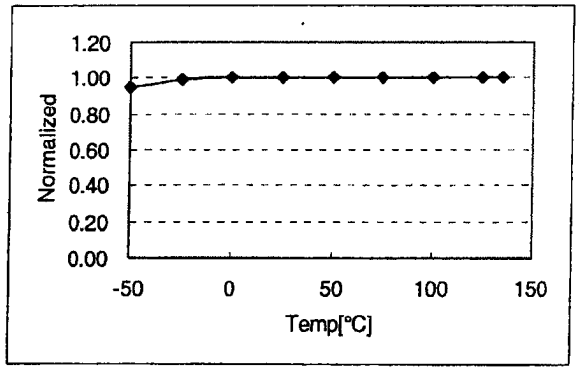
10. Pulse test : Pulse width ≤ 300µs, duty ≤ 2%
11. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics (Control Part)

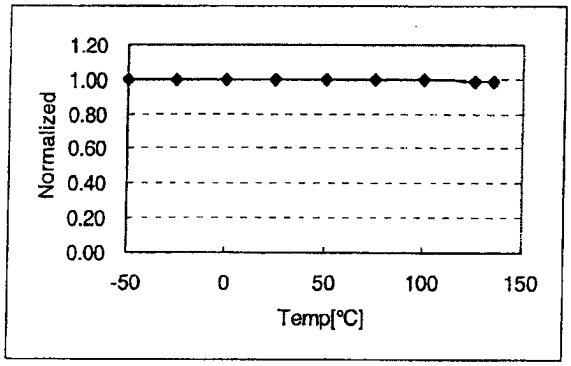
(These characteristic graphs are normalized at T_A = 25°C)



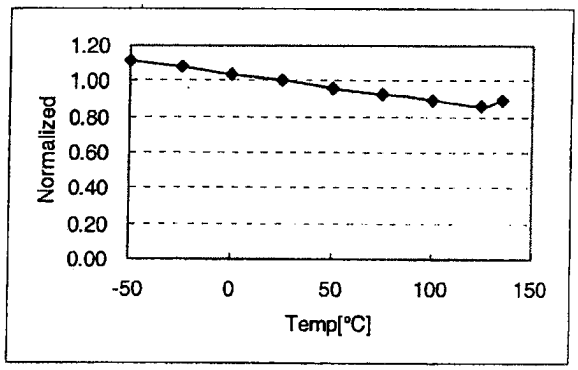
Operating Frequency (fosc) vs. T_A



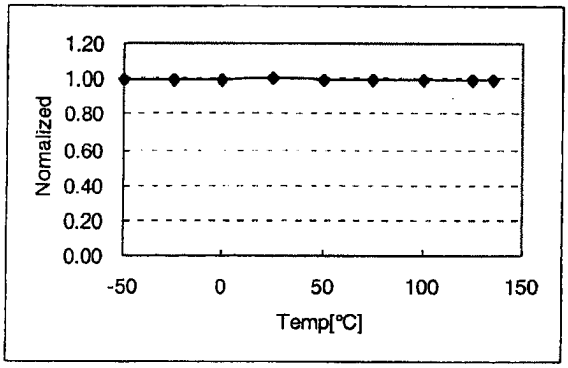
Frequency Modulation (Δf_{MOD}) vs. T_A



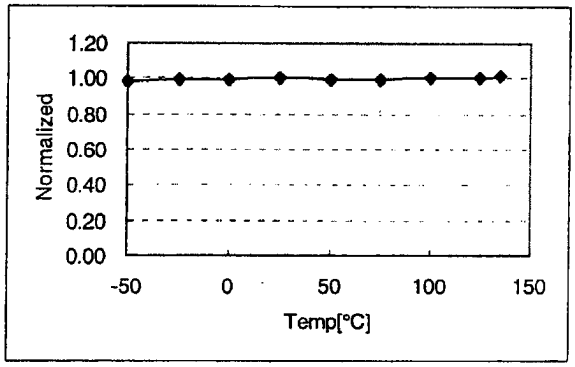
Maximum Duty Cycle (D_{MAX}) vs. T_A



Operating Supply Current (I_{OP}) vs. T_A

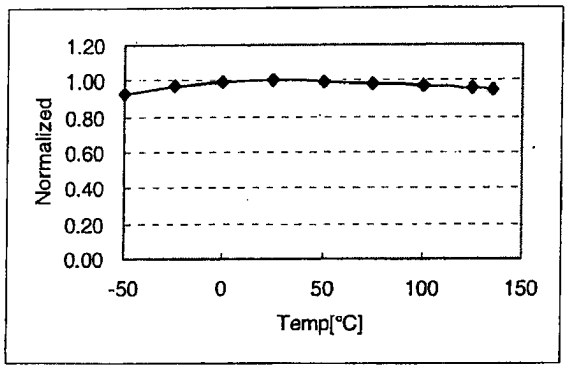


Start Threshold Voltage (V_{START}) vs. T_A

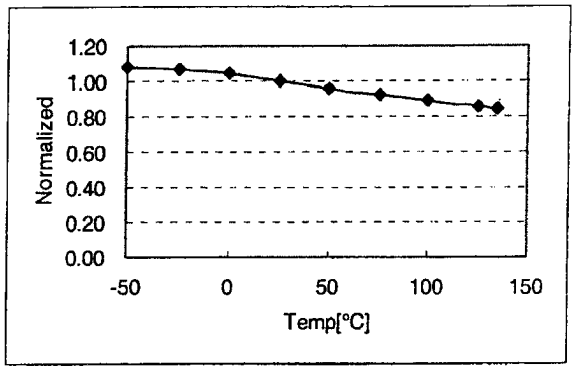


Stop Threshold Voltage (V_{STOP}) vs. T_A

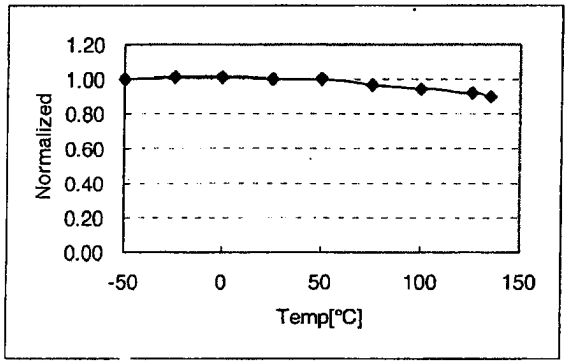
Typical Performance Characteristics (Continued)



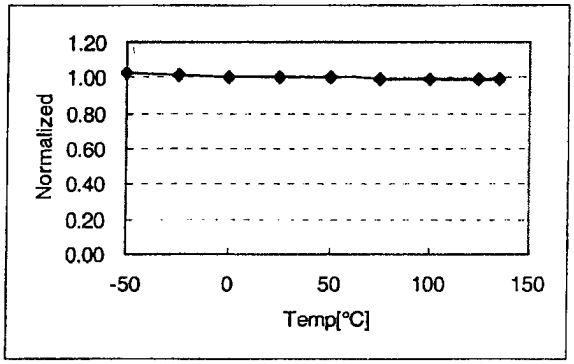
Feedback Source Current (I_{FB}) vs. T_A



Start Up Charging Current (I_{CH}) vs. T_A



Peak Current Limit (I_{LIM}) vs. T_A



Over Voltage Protection (V_{OVP}) vs. T_A

Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™) the Vstr pin required an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off 10ms after the supply voltage, Vcc, goes above 12V. The source turns back on if Vcc drops below 8V.

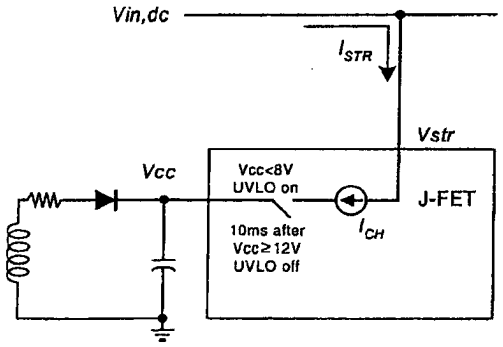


Figure 4. High Voltage Current Source

2. Feedback Control: The 700V FPS series employs current mode control, as shown in Figure 5. An optocoupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor of Sense FET plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and thereby reduces the duty cycle. This typically happens when the input voltage increases or the output load decreases.

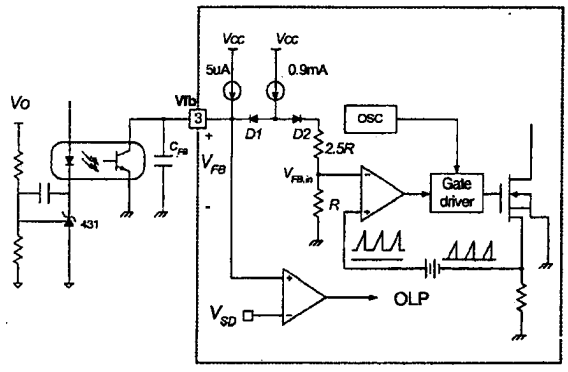
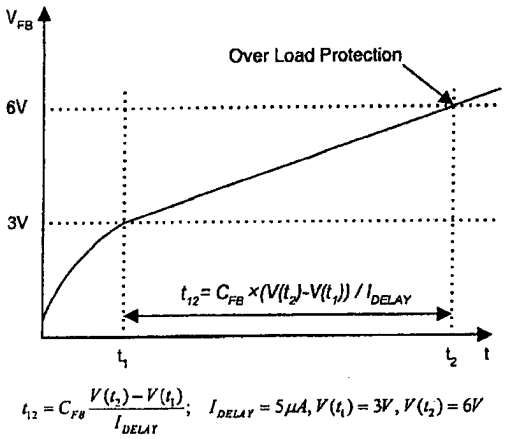


Figure 5. Pulse Width Modulation (PWM) Circuit

3. Leading Edge Blanking (LEB): When the internal Sense FET is turned on; the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a Leading Edge Blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits: The FPS has several protective functions such as Over Load Protection (OLP), Over Voltage Protection (OVP), Under Voltage Lock Out (UVLO), and Thermal Shut Down (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, V_{STOP} (typically 8V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage, V_{START} (typically 12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the Over Load Protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its nominal voltage. This reduces the current through the optocoupler LED, which also reduces the optocoupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to slowly charge Cfb up to Vcc. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated as shown in Figure 6. The shutdown delay time is the time required to charge Cfb from 3V to 6V with 5μA current source.



$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}};\quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 6V$$

Figure 6. Over Load Protection (OLP)

4.2 Thermal Shutdown (TSD): The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Over Voltage Protection (OVP): In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the optocoupler transistor becomes almost zero (refer to Figure 5). Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation; an Over Voltage Protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

5. Soft Start: The FPS has an internal soft start circuit that slowly increases the Sense FET current after startup as shown in Figure 7. The typical soft start time is 10ms, where progressive increments of the Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

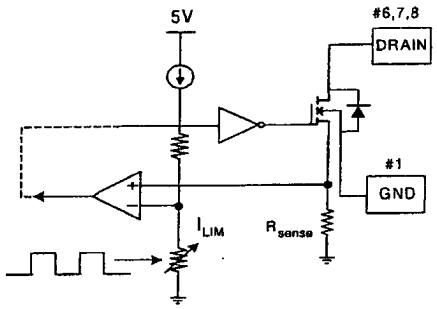


Figure 7. Soft Start Function

6. Burst Operation: In order to minimize power dissipation in standby mode, the FPS enters burst mode operation. Feedback voltage decreases as the load decreases and as shown in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (typically 600mV). Switching still continues until the feedback voltage drops below V_{BURL} (typically 400mV). At this point switching stops and the output voltage start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process is repeated. Burst mode operation alternately enables and disables switching of the Sense FET and reduces switching loss in standby mode.

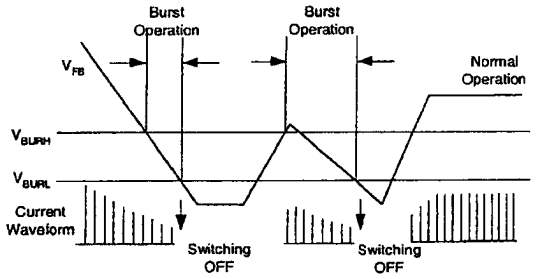


Figure 8. Burst Operation Function

7. Frequency Modulation: Modulating the switching frequency of a switched power supply can reduce EMI. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 9, the frequency changes from 97KHz to 103KHz in 4ms for the 700V FPS series. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

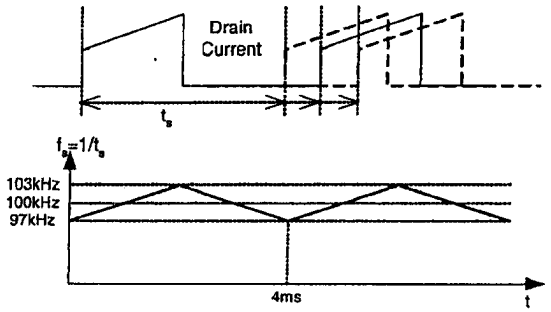


Figure 9. Frequency Modulation Waveform

8. Adjusting Peak Current Limit: As shown in Figure 10, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

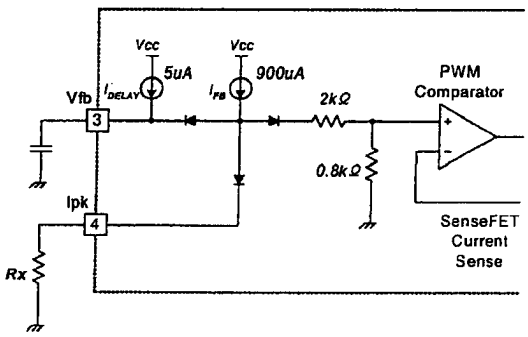


Figure 10. Peak Current Limit Adjustment

For example, FSDH0270RNB has a typical Sense FET peak current limit (I_{LIM}) of 0.9A. I_{LIM} can be adjusted to 0.6A by inserting Rx between the Ipk pin and the ground. The value of the Rx can be estimated by the following equations:

0.9A : 0.6A = 2.8kΩ : XkΩ,

X = Rx || 2.8kΩ.

(X represents the resistance of the parallel network)

Application Tips

1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise depending on the load condition. Here are three methods to reduce noise:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. Glue or varnish can also can crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. Another consideration is to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4KHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4KHz. When the fundamental frequency of noise is located in this range, the noise sounds louder although the noise intensity level is identical. Refer to Figure 11.

When FPS acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4KHz, adjusting the feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor (C_F), optocoupler supply resistor (R_D) and feedback capacitor (C_B) and decrease a feedback gain resistor (R_F) as shown in Figure 12.

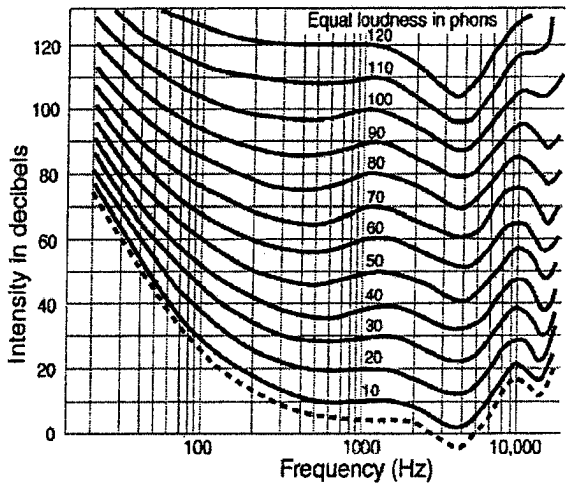


Figure 11. Equal Loudness Curves

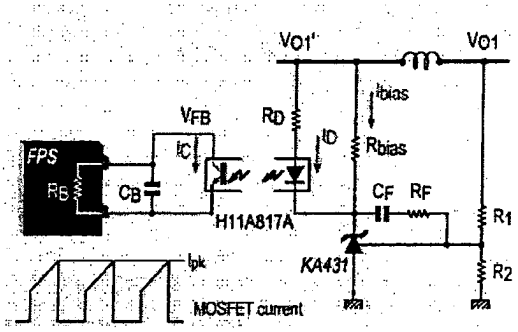


Figure 12. Typical Feedback Network of FPS

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137:Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Typical Application Circuit

Application	Output power	Input voltage	Output Voltage (Max current)
PC Auxiliary Power Supply (Using FSDH0270RNB)	15W	Universal input (85–265 Vac)	5V (3A)

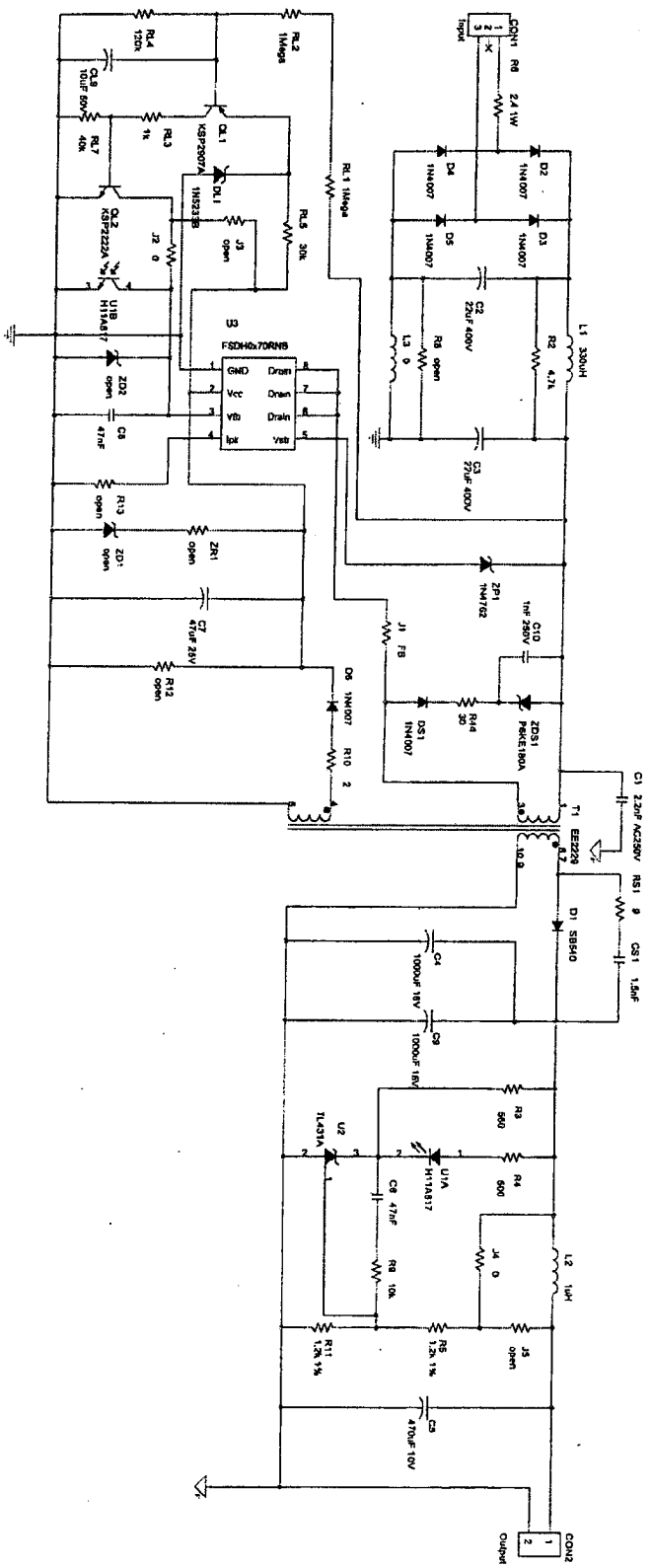
Features

- High efficiency (> 78% at 115 Vac and 230 Vac input)
- Low standby mode power consumption (< 0.8W at 230 Vac input and 0.5W load)
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft-start (10ms)
- Line UVLO function can be achieved using external component

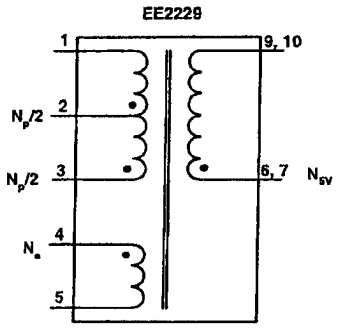
Key Design Notes

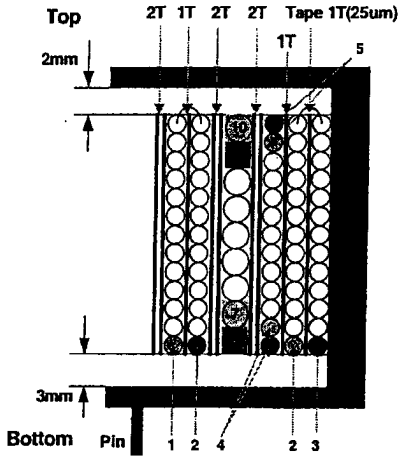
- The delay time for overload protection is designed to be about 30ms with C8 of 47nF. If faster/slower triggering of OLP is required, C8 can be changed to a smaller/larger value (e.g. 100nF for about 60ms).
- ZP1, DL1, RL1, RL2, RL3, RL4, RL5, RL7, QL1, QL2, and CL9 build a Line Under Voltage Lock Out block (UVLO). The zener voltage of ZP1 determines the input voltage which makes FPS turn on. RL5 and DL1 provide a reference voltage from V_{CC}. If the input voltage divided by RL1, RL2, and RL4 is lower than the zener voltage of DL1, QL1 and QL2 turn on and pull down Vfb to ground.
- This evaluation board and corresponding test report can be provided.

1. Schematic


CON1
Input
R6
2.4 1W
D4
1N4007
D2
1N4007
D5
1N4007
D3
1N4007
C2
22uF 400V
L3
0
R3
open
R2
4.7k
L1
330uH
C3
27uF 400V
U3
FSDH0x70RNB
GND
Vcc
VB
Ipk
Drain
Drain
Drain
Vstr
U1B
H11A817
ZD2
open
C6
47nF
R13
open
ZD1
open
ZR1
open
C7
47uF 25V
R12
open
ZP1
1N4762
J1
FB
C10
1nF 250V
D6
1N4007
R10
2
D51
1N4007
R14
30
ZD51
P6KE180A
T1
EE2228
C1
2.2nF AC250V
RS1
0
D1
SB540
CS1
1.5nF
C4
1000uF 16V
C9
1000uF 16V
R3
560
U2
TL431A
U1A
H11A817
R4
560
C8
47nF
R8
10k
J4
0
L2
1uH
R11
1.2k 1%
R5
1.2k 1%
J5
open
C5
470uF 10V
CON2
Output

2. Transformer Schematic Diagram





3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 1 Layers				
N_a	4 → 5	0.25φ × 2	22	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{5V}	6, 7 → 9, 10	0.65φ × 2	8	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				

4. Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1–3	1.20mH ± 5%	100kHz, 1V
Leakage	1–3	< 30μH Max	Short all other pins

5. Core & Bobbin

Core: EE2229 (Material: PL-7, Ae = 35.7 mm^2)

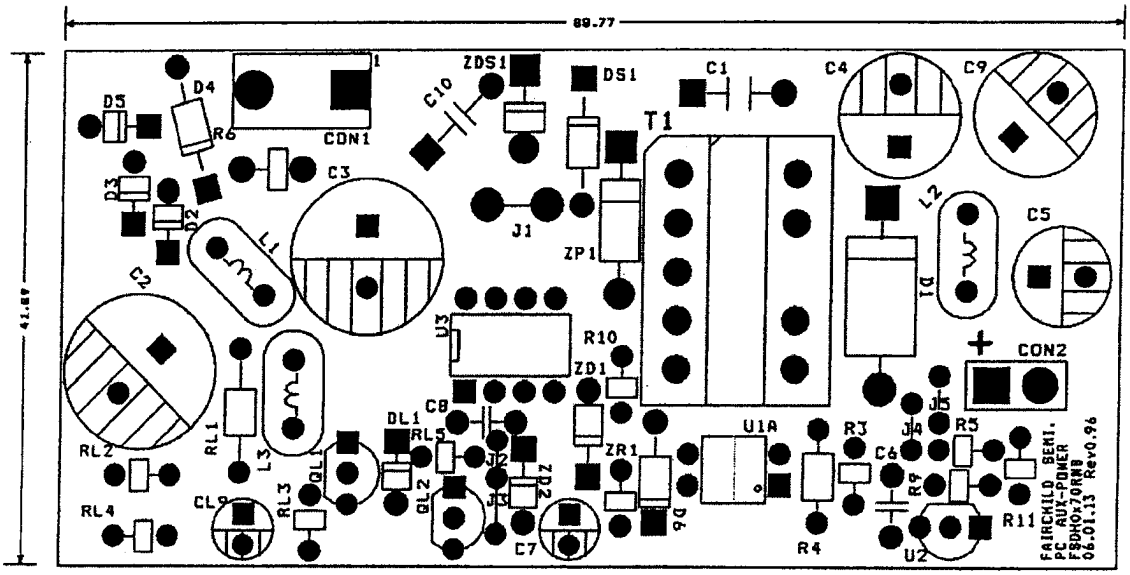
Bobbin: 10 pin

6. Demo Circuit Part List

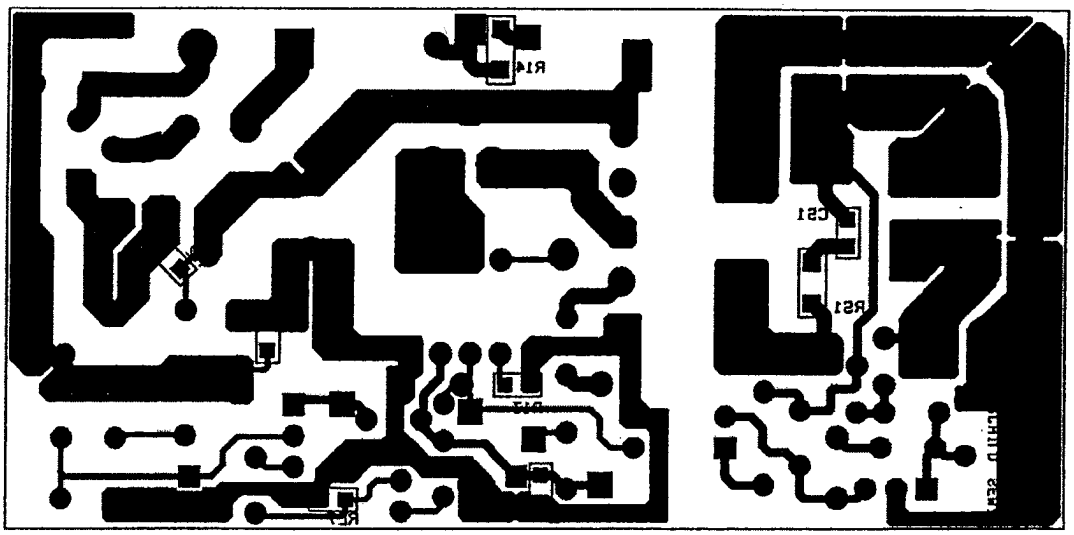
Part Number	Value	Quantity	Description (Manufacturer)
C6, C8	47nF	2	Ceramic Capacitor
C1	2.2nF (250V)	1	AC Ceramic Capacitor
C10	1nF (250V)	1	Film Capacitor
CS1	1.5nF (50V)	1	SMD Ceramic Capacitor
C2, C3	22μF (400V)	2	Low Impedance Electrolytic Capacitor KMX series (Samyoung Elec.)
C4, C9	1000μF (16V)	2	Low ESR Electrolytic Capacitor NXC series (Samyoung Elec.)
C5	470μF (10V)	1	Low ESR Electrolytic Capacitor NXC series (Samyoung Elec.)
C7	47μF (25V)	1	General Electrolytic Capacitor
CL9	10μF (50V)	1	General Electrolytic Capacitor
L1	330μH	1	Inductor
L2	1μH	1	Inductor
R6	2.4 (1W)	1	Fusible Resistor
J1	FB	1	Ferrite Beads
J2, J4, L3	0	3	Jumper
R2	4.7k	1	Resistor
R3	560	1	Resistor
R4	500	1	Resistor
R5, R11	1.2k(1%)	2	Resistor
R9	10k	1	Resistor
R10	2	1	Resistor
R14	30	1	Resistor
RL3	1k	1	Resistor
RL1, RL2	1 Mega	2	Resistor
RL4	120k	1	Resistor
RL5	30k	1	Resistor
RL7	40k	1	Resistor
RS1	9	1	Resistor
U1	H11A817	1	Optocoupler (Fairchild Semiconductor)
U2	TL431A	1	Shunt Regulator (Fairchild Semiconductor)
U3	FSDH0x70RNB	1	FPS™ (Fairchild Semiconductor)
QL1	KSP2907A	1	PNP Transistor (Fairchild Semiconductor)
QL2	KSP2222A	1	NPN Transistor (Fairchild Semiconductor)
D2, D3, D4, D5, D6, DS1	1N4007	6	Diode (Fairchild Semiconductor)
D1	SB540	1	Schottky Diode (Fairchild Semiconductor)
DL1	1N5233B	1	Zener Diode (Fairchild Semiconductor)
ZP1	1N4762	1	Zener Diode
ZDS1	P6KE180A	1	TVS (Fairchild Semiconductor)
T1	EE2229	1	PL-7 Core (Samwha Elec.)

7. Layout

7.1 Top image of PCB



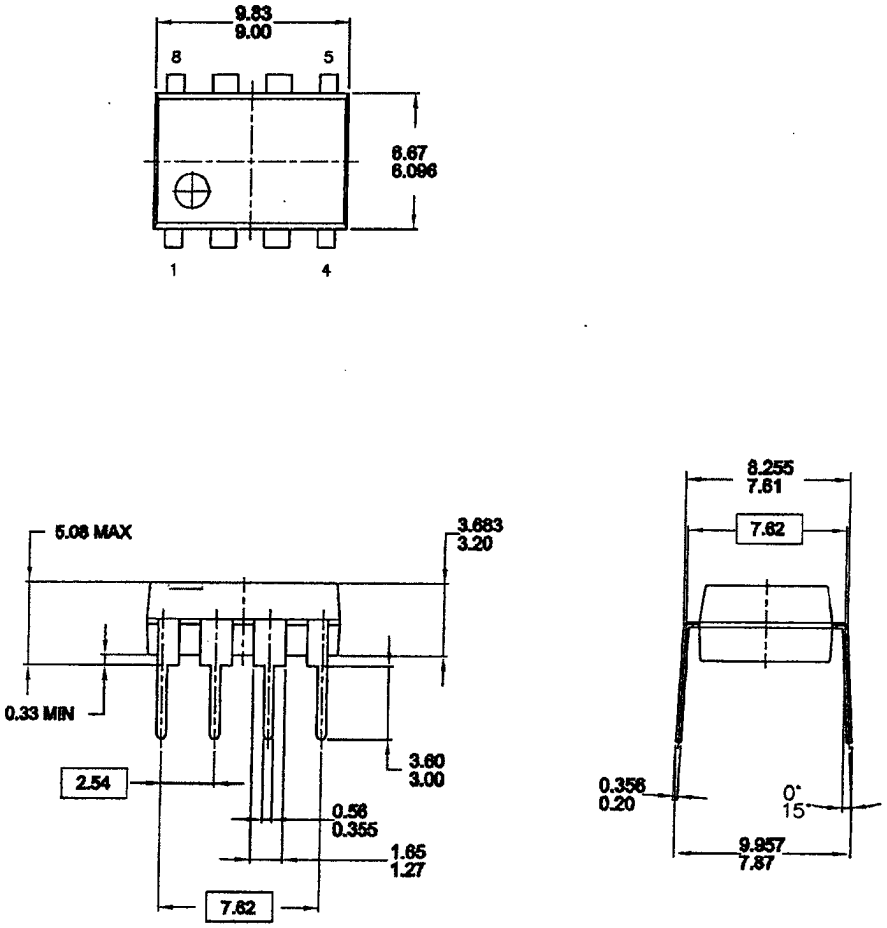
7.2 Bottom image of PCB



Package Dimensions

8-Pin DIP

Dimemsions in millimeters



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C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

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Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOME™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I²C™	MSXPro™	RapidConnect™	UHC™
E²CMOS™	*i-Lo*™	OCX™	µSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I18

PIF 145197 – PIF 145198

THESE NUMBERS INTENTIONALLY OMITTED

EXHIBIT 3

FAIRCHILD SEMICONDUCTOR®

September 2007

FSQ0365, FSQ0265, FSQ0165, FSQ321, FSQ311 Green Mode Fairchild Power Switch (FPS™) for Valley Switching Converter - Low EMI and High Efficiency

Features

- Optimized for Valley Switching (VSC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage SenseFET (650V)
- Built-in Soft-Start (15ms)

Applications

- Power Supply for DVP Player and DVD Recorder, Set-Top Box
- Adapter
- Auxiliary Power Supply for PC, LCD TV, and PDP TV

Related Application Notes

- AN-4137, AN-4141, AN-4147, AN-4150 (Flyback)
- AN-4134 (Forward)

Description

A Valley Switching Converter generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ-series is an integrated Pulse-Width Modulation (PWM) controller and SenseFET specifically designed for valley switching operation with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout, Leading Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry.

Compared with discrete MOSFET and PWM controller solutions, the FSQ-series reduces total cost, component count, size and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of valley switching fly-back converters.

FPS™ is a trademark of Fairchild Semiconductor Corporation.

Ordering Information

Product Number[5]	PKG.	Operating Temp.	Current Limit	$R_{DS(ON)}$ Max.	Maximum Output Power[1]				Replaces Devices
					230VAC±15%[2]		85-265VAC		
					Adapter[3]	Open-Frame[4]	Adapter[3]	Open-Frame[4]	
FSQ311	8-DIP	-40 to +85C	0.6A	19Ω	7W	10W	6W	8W	FSDL321 FSDM311
FSQ311L	8-LSOP								
FSQ321	8-DIP	-40 to +85°C	0.6A	19Ω	8W	12W	7W	10W	FSDL321 FSDM311
FSQ321L	8-LSOP								
FSQ0165RN	8-DIP	-40 to +85°C	0.9A	10Ω	10W	15W	9W	13W	FSDL0165RN
FSQ0165RL	8-LSOP								
FSQ0265RN	8-DIP	-40 to +85°C	1.2A	6Ω	14W	20W	11W	16W	FSDM0265RN FSDM0265RNB
FSQ0265RL	8-LSOP								
FSQ0365RN	8-DIP	-40 to +85°C	1.5A	4.5Ω	17.5W	25W	13W	19W	FSDM0365RN FSDM0365RNB
FSQ0365RL	8-LSOP								

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler. The maximum power with CCM operation.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. Pb-free package per JEDEC J-STD-020B.

Typical Circuit

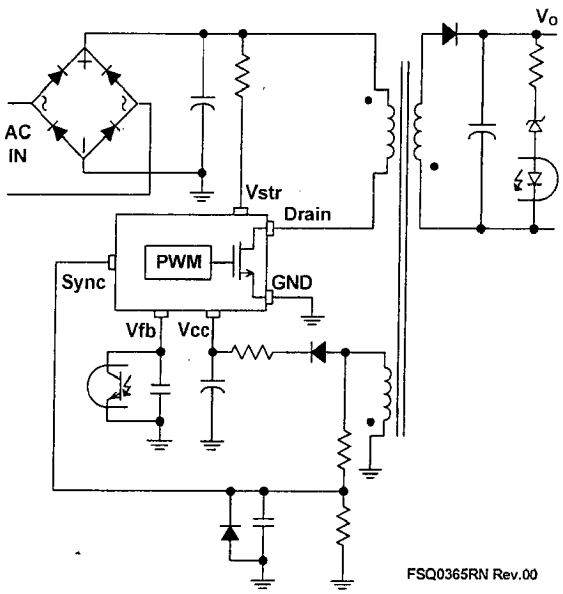


Figure 1. Typical Flyback Application

Internal Block Diagram

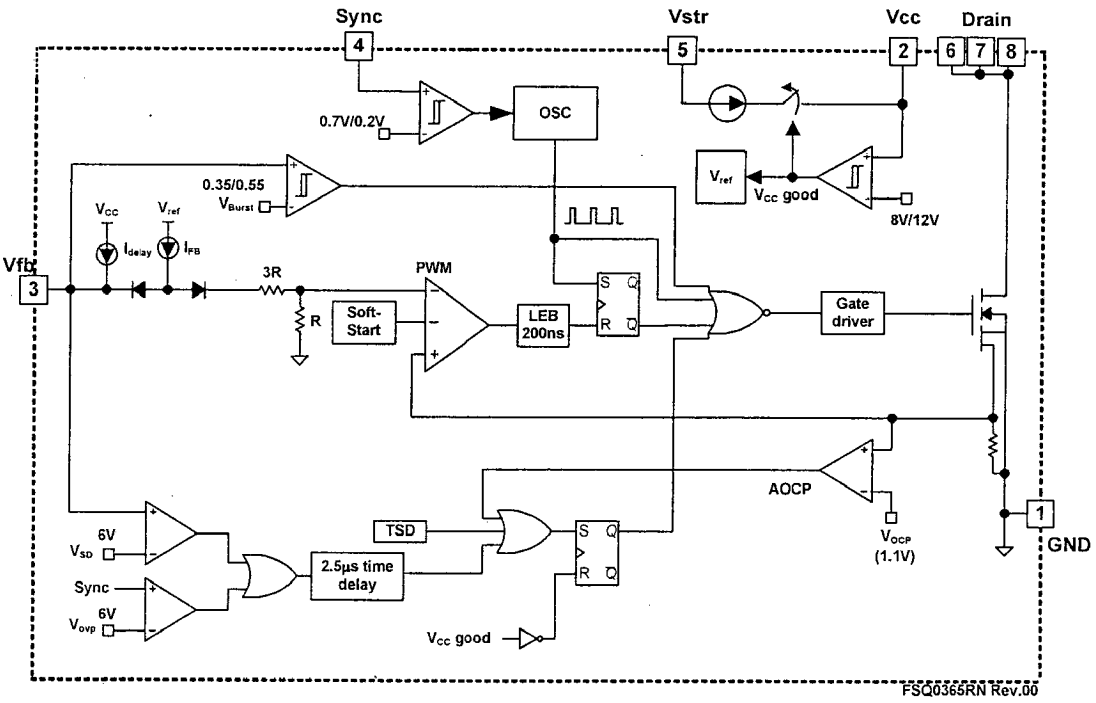


Figure 2. Functional Block Diagram

Pin Configuration

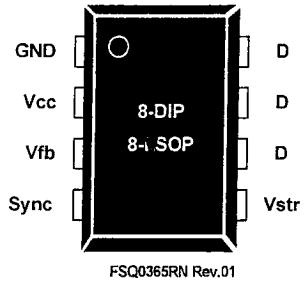


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	SenseFET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram Section). It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. There is a time delay while charging external capacitor Cfb from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	Sync	This pin is internally connected to the sync-detect comparator for valley switching. Typically the voltage of the auxiliary winding is used as Sync input voltage and external resistors and capacitor are needed to make time delay to match valley point. The threshold of the internal sync comparator is 0.7V/0.2V.
5	Vstr	This pin is connected to the rectified AC line voltage source. At start-up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6,7,8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Characteristic		Min.	Max.	Unit
V_{STR}	V_{str} Pin Voltage		500		V
V_{DS}	Drain Pin Voltage		650		V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	9.0	V
V_{Sync}	Sync Pin Voltage Range		-0.3	9.0	V
I_{DM}	Drain Current Pulsed(6)	FSQ0365		12	A
		FSQ0265		8	
		FSQ0165		4	
		FSQ321/311		1.5	
E_{AS}	Single Pulsed Avalanche Energy(7)	FSQ0365		230	mJ
		FSQ0265		140	
		FSQ0165		50	
		FSQ321/311		10	
P_D	Total Power Dissipation			1.5	W
T_J	Recommended Operating Junction Temperature		-40	Internally limited	°C
T_A	Operating Ambient Temperature		-40	85	°C
T_{STG}	Storage Temperature		-55	150	°C
ESD	Human Body Model(8)		CLASS1 C		
	Machine Model(8)		CLASS B		

Notes:

6. Repetitive rating: Pulse width limited by maximum junction temperature.
7. L=51mH, starting T_J=25°C.
8. Meets JEDEC standards JESD22-A114 and JESD22-A115.

Thermal Impedance

Symbol	Parameter	Value	Unit
8-DIP(9)			
θ_{JA}(10)	Junction-to-Ambient Thermal Resistance	80	°C/W
θ_{JC}(11)	Junction-to-Case Thermal Resistance	20	
θ_{JT}(12)	Junction-to-Top Thermal Resistance	35	

Notes:

9. All items are tested with the standards JESD 51-2 and 51-10 (DIP).
10. Free-standing, with no heat-sink, under natural convection.
11. Infinite cooling condition - refer to the SEMI G30-88.
12. Measured on the package top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SenseFET Section							
BV_{DSS}	Drain Source Breakdown Voltage		V_{CC} = 0V, I_D = 100μA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 560V			100	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[13]	FSQ0365	T_J = 25°C, I_D = 0.5A		3.5	4.5	Ω
		FSQ0265			5.0	6.0	
		FSQ0165			8.0	10.0	
		FSQ321/311			14.0	19.0	
C_{SS}	Input Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		315		pF
		FSQ0265			550		
		FSQ0165			250		
		FSQ321/311			162		
C_{OSS}	Output Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		47		pF
		FSQ0265			38		
		FSQ0165			25		
		FSQ321/311			18		
C_{RSS}	Reverse Transfer Capacitance	FSQ0365	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		9.0		pF
		FSQ0265			17.0		
		FSQ0165			10.0		
		FSQ321/311			3.8		
$t_{d(on)}$	Turn-On Delay Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		11.2		ns
		FSQ0265			20.0		
		FSQ0165			12.0		
		FSQ321/311			9.5		
t_r	Rise Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		34		ns
		FSQ0265			15		
		FSQ0165			4		
		FSQ321/311			19		
$t_{d(off)}$	Turn-Off Delay Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		28.2		ns
		FSQ0265			55.0		
		FSQ0165			30.0		
		FSQ321/311			33.0		
t_f	Fall Time	FSQ0365	V_{DD} = 350V, I_D = 25mA		32		ns
		FSQ0265			25		
		FSQ0165			10		
		FSQ321/311			42		
Control Section							
$t_{ON.MAX1}$	Maximum On Time1	All but Q321	T_J = 25°C	10.5	12.0	13.5	μs
$t_{ON.MAX2}$	Maximum On Time2	Q321	T_J = 25°C	6.35	7.06	7.77	μs
t_{B1}	Blanking Time1	All but Q321		13.2	15.0	16.8	μs
t_{B2}	Blanking Time2	Q321		7.5	8.2		μs

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
t_W	Detection Time Window		T_J = 25°C, V_{sync} = 0V		3.0		µs
f_{S1}	Initial Switching Freq.1	All but Q321		50.5	55.6	61.7	kHz
f_{S2}	Initial Switching Freq.2	Q321		84.0	89.3	95.2	kHz
Δf_S	Switching Frequency Variation(14)		-25°C < T_J < 85°C		±5	±10	%
I_{FB}	Feedback Source Current		V_{FB} = 0V	700	900	1100	µA
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage		After turn-on	11	12	13	V
V_{STOP}				7	8	9	V
$t_{S/S1}$	Internal Soft-Start Time1	All but Q321	With free-running frequency		15		ms
$t_{S/S2}$	Internal Soft-Start Time2	Q321	With free-running frequency		10		ms
Burst Mode Section							
V_{BURH}	Burst-Mode Voltage		T_J = 25°C, t_{PD} = 200ns(15)	0.45	0.55	0.65	V
V_{BURL}				0.25	0.35	0.45	V
$V_{BUR(HYS)}$					200		mV
Protection Section							
I_{LIM}	Peak Current Limit	FSQ0365	T_J = 25°C, di/dt = 240mA/µs	1.32	1.50	1.68	A
		FSQ0265	T_J = 25°C, di/dt = 200mA/µs	1.06	1.20	1.34	
		FSQ0165	T_J = 25°C, di/dt = 175mA/µs	0.8	0.9	1.0	
		FSQ321	T_J = 25°C, di/dt = 125mA/µs	0.53	0.60	0.67	
		FSQ311	T_J = 25°C, di/dt = 112mA/µs	0.53	0.60	0.67	
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	4	5	6	µA
t_{LEB}	Leading-Edge Blanking Time(14)				200		ns
V_{OVP}	Over-Voltage Protection		V_{CC} = 15V, V_{FB} = 2V	5.5	6.0	6.5	V
t_{OVP}	Over-Voltage Protection Blanking Time			2	3	4	µs
T_{SD}	Thermal Shutdown Temperature(14)			125	140	155	°C
Sync Section							
V_{SH}	Sync Threshold Voltage			0.55	0.70	0.85	V
V_{SL}				0.14	0.20	0.26	V
t_{Sync}	Sync Delay Time(14)(16)				300		ns
Total Device Section							
I_{OP}	Oper. Supply Current (Control Part Only)		V_{CC} = 15V	1	3	5	mA
I_{START}	Start Current		V_{CC} = V_{START} - 0.1V (before V_{CC} reaches V_{START})	270	360	450	µA
I_{CH}	Start-up Charging Current		V_{CC} = 0V, V_{STR} = min. 40V	0.65	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage				26		V

Notes:

13. Pulse test: Pulse-Width=300µs, duty=2%
14. Though guaranteed, it is not 100% tested in production.
15. Propagation delay in the control IC.
16. Includes gate turn-on time.

Comparison Between FSDM0x65RNB and FSQ-Series

Function	FSDM0x65RNB	FSQ-Series	FSQ-Series Advantages
Operation method	Constant frequency PWM	Valley switching operation	■ Improved efficiency by valley switching ■ Reduced EMI noise
EMI reduction	Frequency modulation	Valley switching & inherent frequency modulation	■ Reduce EMI noise by two ways
Burst-mode operation	Fixed burst peak	Advanced burst-mode	■ Improved standby power by valley switching also in burst-mode ■ Because the current peak during burst operation is dependent on V_{FB}, it is easier to solve audible noise
Protection		AOCP	■ Improved reliability through precise abnormal over-current protection

Typical Performance Characteristics

These characteristic graphs are normalized at T_A= 25°C.

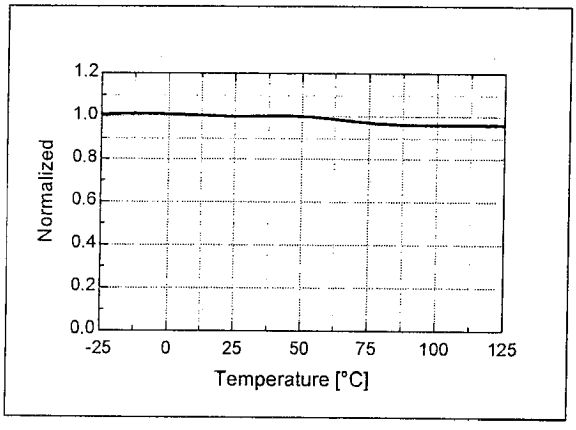


Figure 4. Operating Supply Current (I_{OP}) vs. T_A

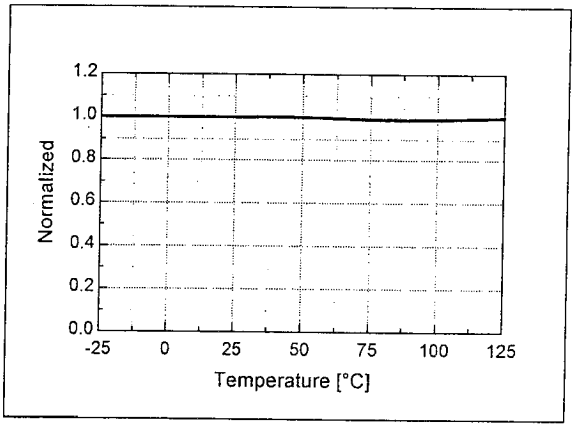


Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

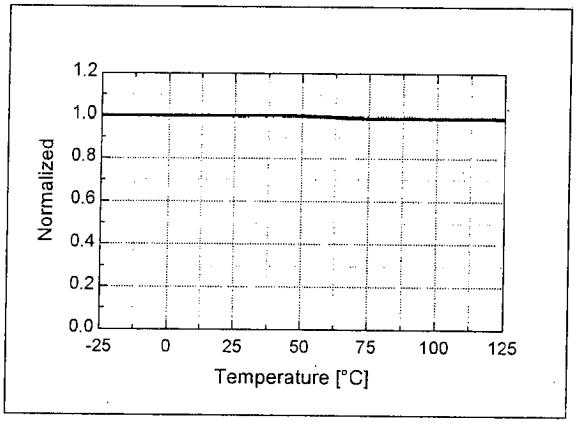


Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

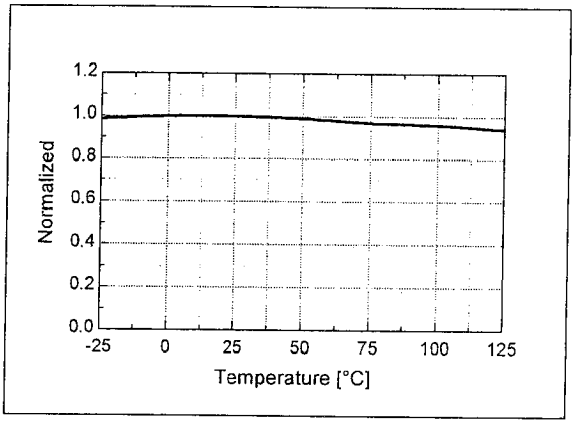


Figure 7. Start-up Charging Current (I_{CH}) vs. T_A

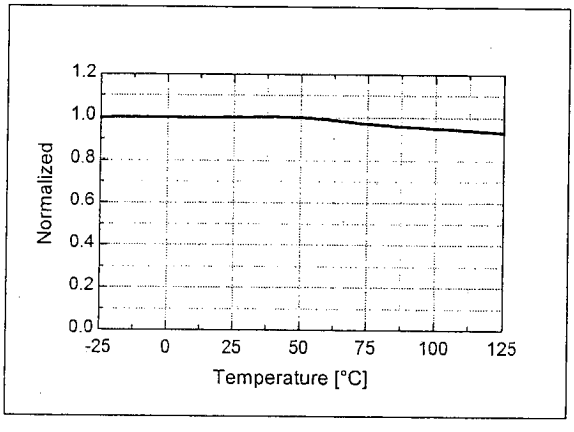


Figure 8. Initial Switching Frequency (f_S) vs. T_A

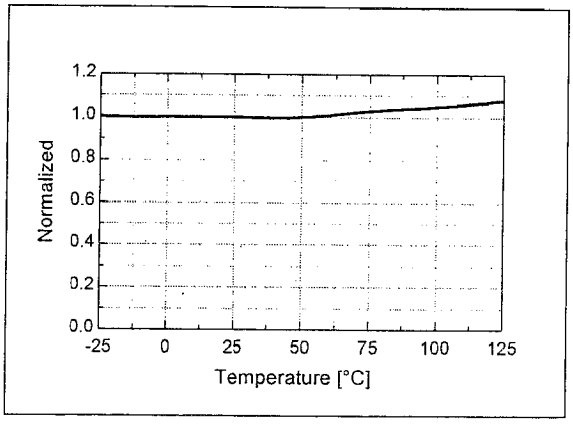


Figure 9. Maximum On Time ($t_{ON.MAX}$) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

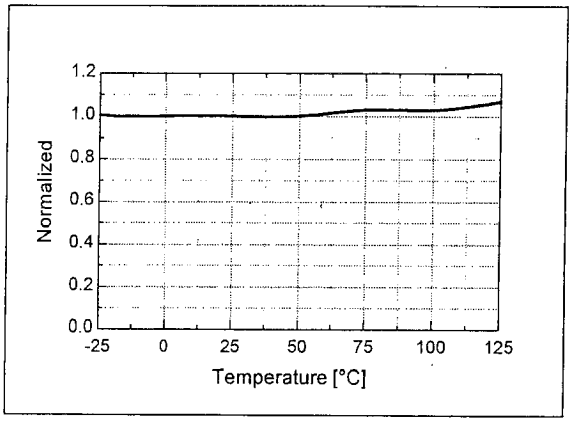


Figure 10. Blanking Time (t_B) vs. T_A

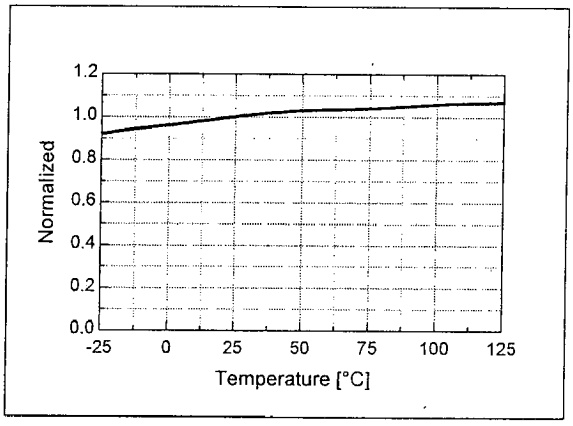


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

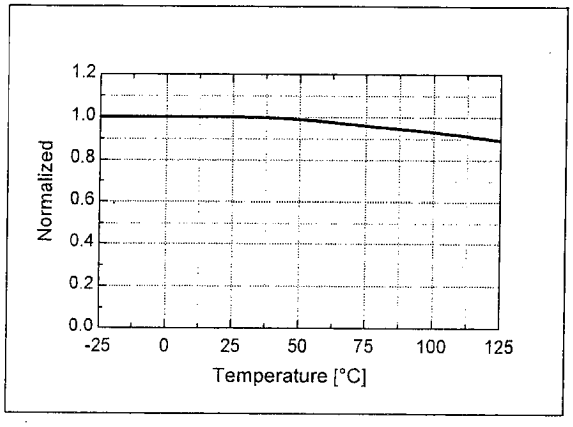


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

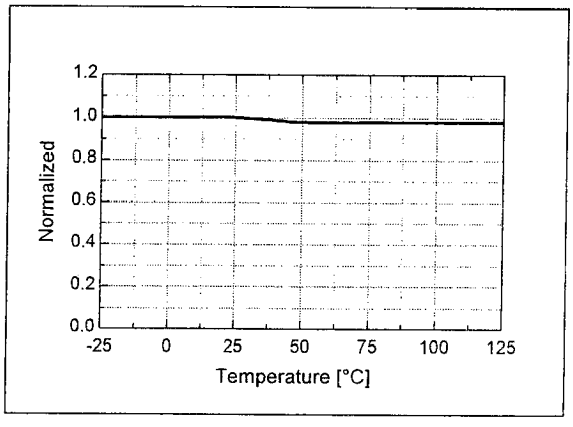


Figure 13. Burst-Mode High Threshold Voltage (V_{burh}) vs. T_A

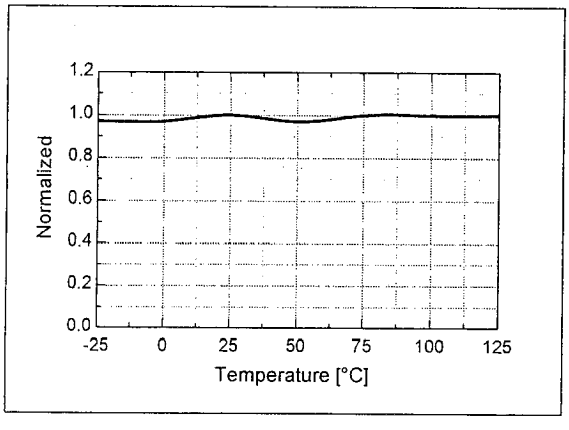


Figure 14. Burst-Mode Low Threshold Voltage (V_{burl}) vs. T_A

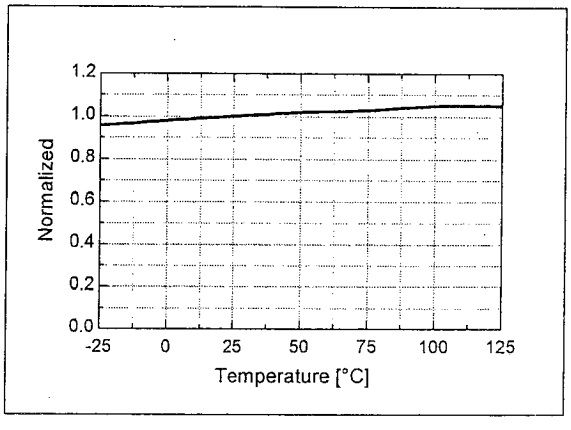


Figure 15. Peak Current Limit (I_{LIM}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

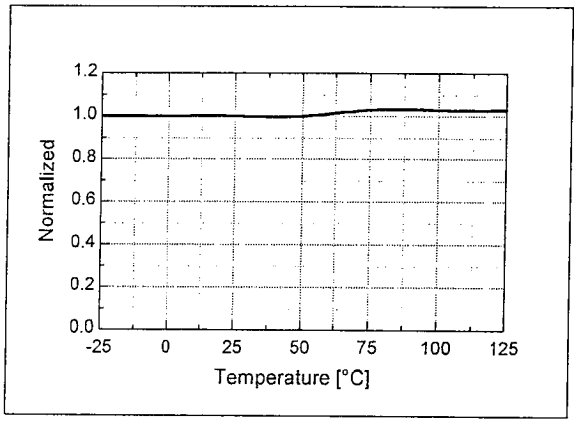


Figure 16. Sync High Threshold Voltage (V_{SH}) vs. T_A

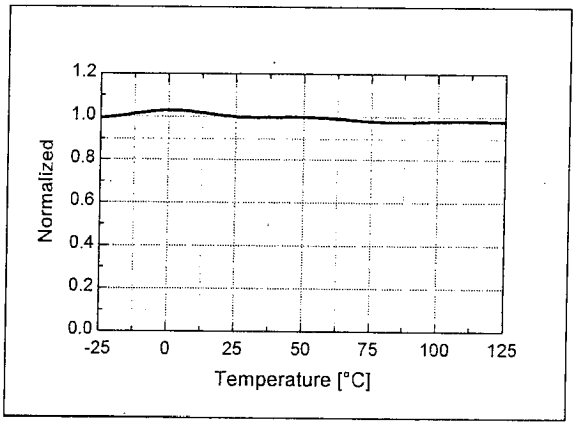


Figure 17. Sync Low Threshold Voltage (V_{SL}) vs. T_A

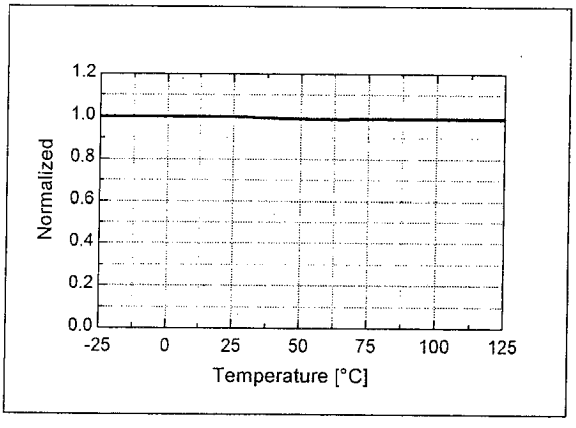


Figure 18. Shutdown Feedback Voltage (V_{SD}) vs. T_A

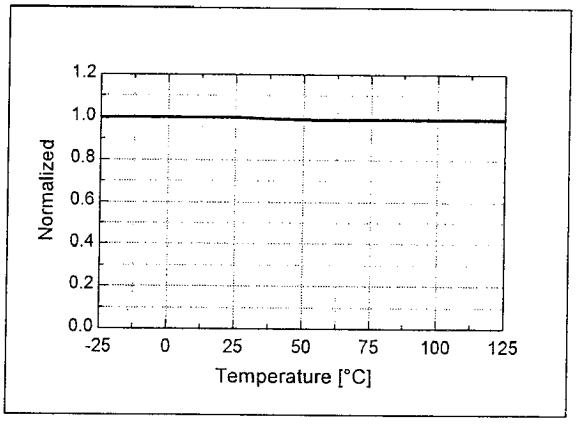


Figure 19. Over-Voltage Protection (V_{OP}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the Vcc pin, as illustrated in Figure 20. When V_{CC} reaches 12V, the FPS begins switching and the internal high-voltage current source is disabled. The FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

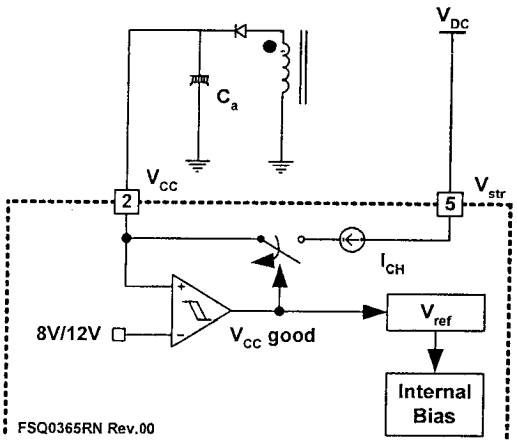


Figure 20. Start-up Circuit

2. Feedback Control: FPS employs current mode control, as shown in Figure 21. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 21. Assuming that the 0.9mA current source flows only through the internal resistor (3R + R = 2.8k), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

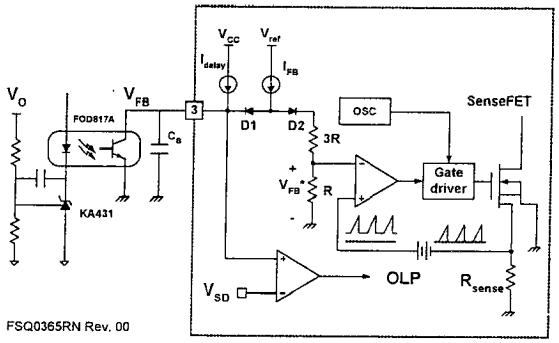


Figure 21. Pulse-Width-Modulation (PWM) Circuit

3. Synchronization: The FSQ-series employs a valley switching technique to minimize the switching noise and loss. The basic waveforms of the valley switching converter are shown in Figure 22. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 22. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 22.

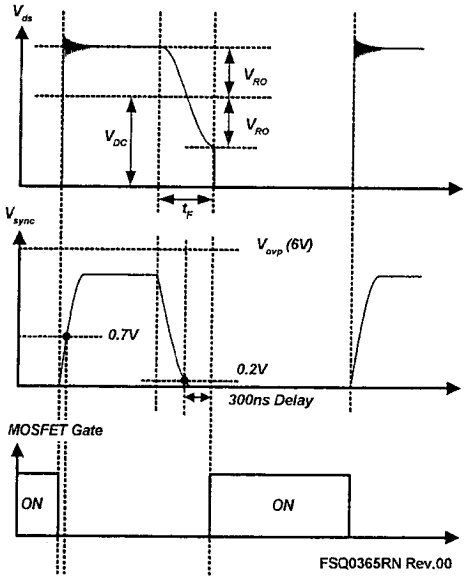


Figure 22. Valley Resonant Switching Waveforms

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 8V, the protection is reset and start-up circuit charges V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12V, the FSQ-series resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

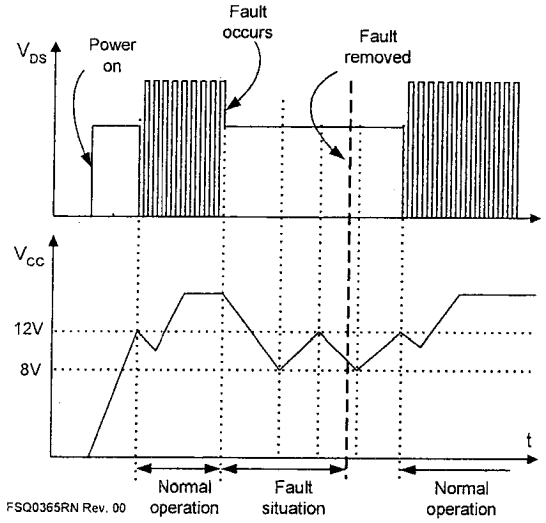


Figure 23. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.8V, D1 is blocked and the 5μA current source starts to charge CB slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 24. The delay time for shutdown is the time required to charge CB from 2.8V to 6V with 5μA. A 20 ~ 50ms delay time is typical for most applications.

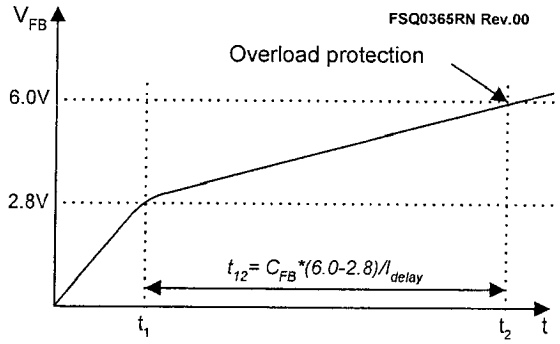


Figure 24. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high-di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has OLP (Overload Protection), it is not enough to protect the FSQ-series in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP (Abnormal Over-Current Protection) circuit as shown in Figure 25. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

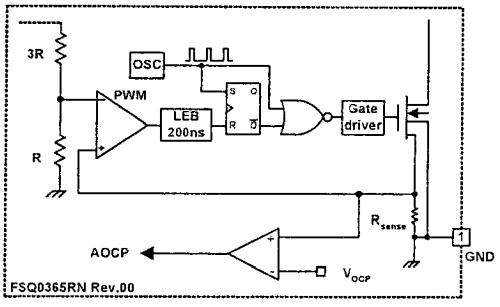


Figure 25. Abnormal Over-Current Protection

4.3 Over-Voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 6V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed below 6V.

4.4 Thermal Shutdown (TSD): The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds ~150°C, the thermal shutdown triggers.

5. Soft-Start: The FPS has an internal soft-start circuit that increases PWM comparator inverting input voltage with the SenseFET current slowly after it starts up. The typical soft-start time is 15ms, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This mode helps prevent transformer saturation and reduces stress on the secondary diode during startup.

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 26, the device automatically enters burst-mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

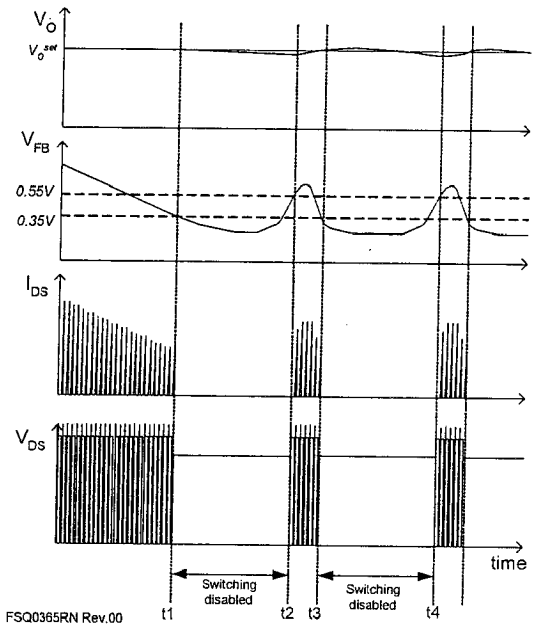


Figure 26. Waveforms of Burst Operation

7. Switching Frequency Limit: To minimize switching loss and EMI (Electromagnetic Interference), the MOSFET turns on when the drain voltage reaches its minimum value in valley switching operation. However, this causes switching frequency to increases at light load conditions. As the load decreases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light-load condition, as well as intermittent switching and audible noise. Because of these problems, the valley switching converter topology has limitations in a wide range of applications.

To overcome this problem, FSQ-series employs a frequency-limit function, as shown in Figures 27 and 28. Once the SenseFET is turned on, the next turn-on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figures 27 and 28 (Cases A, B, and C). If no valley is found during t_W, the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, our devices have a minimum switching frequency of 55kHz and a maximum switching frequency of 67kHz, as shown in Figure 28.

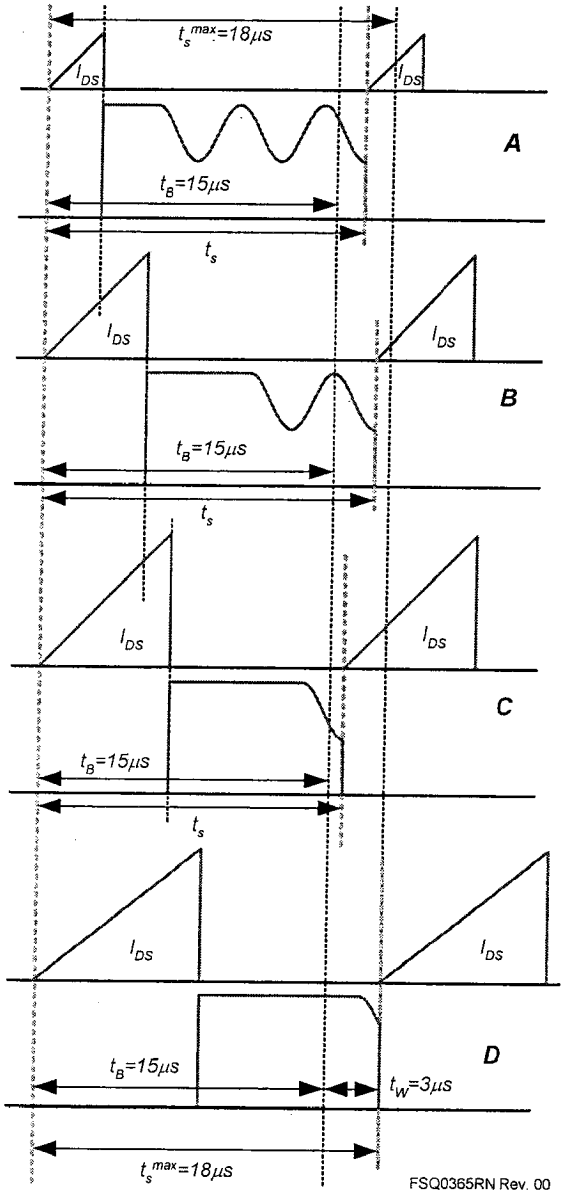


Figure 27. Valley Switching with Limited Frequency

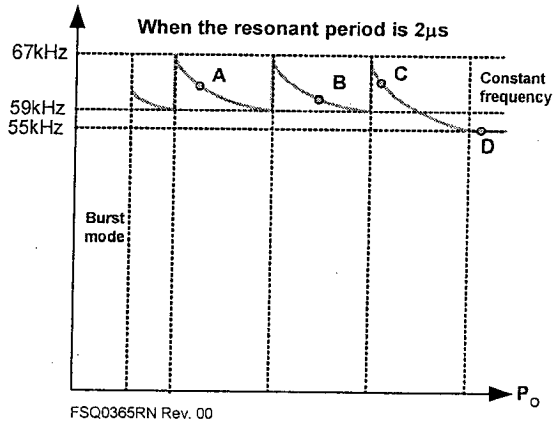


Figure 28. Switching Frequency Range

Typical Application Circuit of FSQ0365RN

Application	FPS Device	Input Voltage Range	Rated Output Power	Output Voltage (Max. Current)
DVD Player Power Supply	FSQ0365RN	85-265V_{AC}	19W	5.1V (1.0A) 3.4V (1.0A) 12V (0.4A) 16V (0.3A)

Features

- High efficiency (>77% at universal input)
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Reduce EMI noise through Valley Switching operation
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C107 of 47nF. If faster/slower triggering of OLP is required, C107 can be changed to a smaller/larger value (eg. 100nF for 60ms).
- The input voltage of V_{sync} must be higher than -0.3V. By proper voltage sharing by R106 & R107 resistors, the input voltage can be adjusted.
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improved surge immunity.

1. Schematic

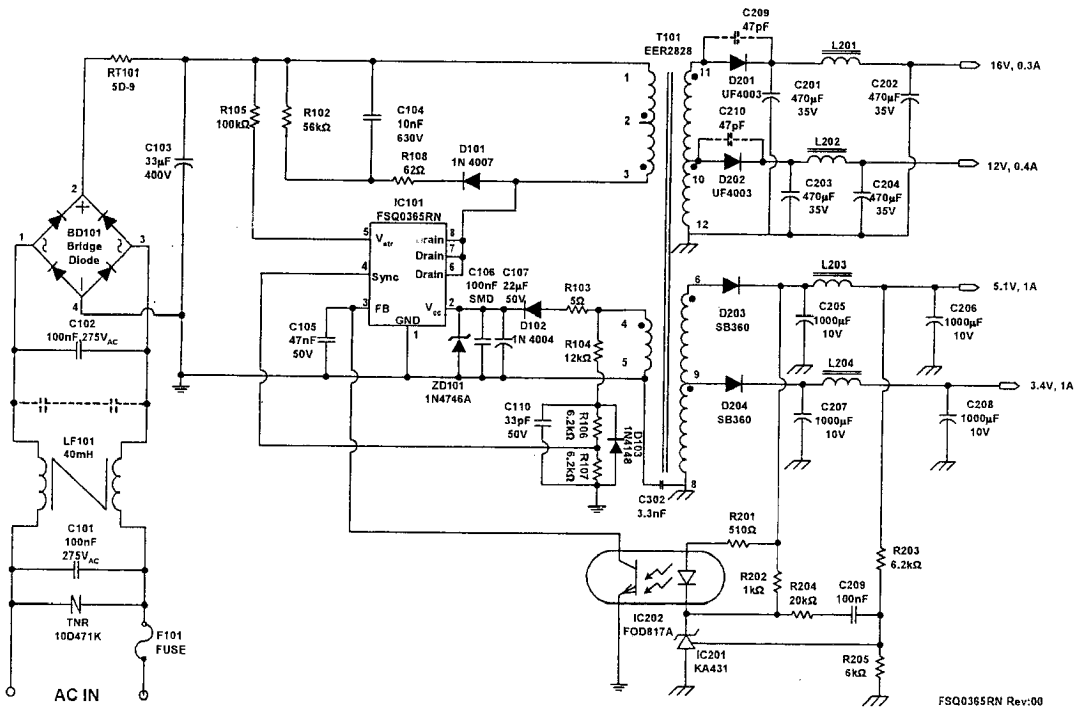


Figure 29. Demo Circuit of FSQ0365RN

2. Transformer

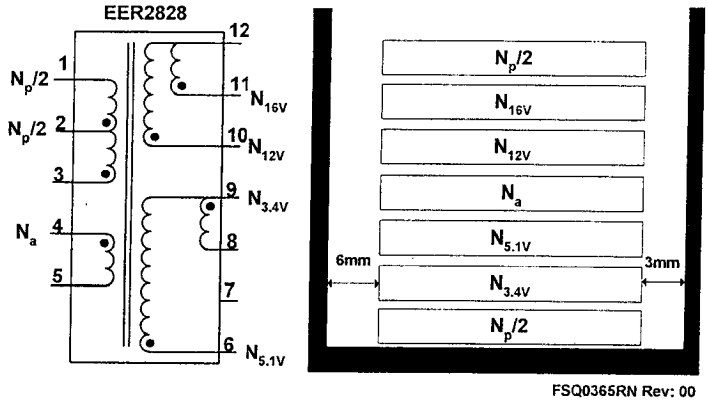


Figure 30. Transformer Schematic Diagram of FSQ0365RN

3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.25^{\phi} \times 1$	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
$N_{3.4V}$	9 → 8	$0.33^{\phi} \times 2$	4	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_{5V}	6 → 9	$0.33^{\phi} \times 1$	2	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_a	4 → 5	$0.25^{\phi} \times 1$	16	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
N_{12V}	10 → 12	$0.33^{\phi} \times 3$	14	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 3 Layers				
N_{16V}	11 → 12	$0.33^{\phi} \times 3$	18	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				
$N_p/2$	2 → 1	$0.25^{\phi} \times 1$	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2 Layers				

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	1.4mH ± 10%	100kHz, 1V
Leakage	1 - 3	25μH Max.	Short all other pins

5. Core & Bobbin

- Core: EER2828 (Ae=86.66mm^2)
- Bobbin: EER2828

6. Demo Board Part List

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R102	56kΩ	1W	L201	10μH	
R103	5Ω	1/2W	L202	10μH	
R104	12kΩ	1/4W	L203	4.9μH	
R105	100kΩ	1/4W	L204	4.9μH	
R106	6.2kΩ	1/4W	**Diode**		
R107	6.2kΩ	1/4W	D101	IN4007	
R108	62Ω	1W	D102	IN4004	
R201	510Ω	1/4W	ZD101	1N4746A	
R202	1kΩ	1/4W	D103	1N4148	
R203	6.2kΩ	1/4W	D201	UF4003	
R204	20kΩ	1/4W	D202	UF4003	
R205	6kΩ	1/4W	D203	SB360	
Capacitor			D204	SB360	
C101	100nF/275V_{AC}	Box Capacitor			
C102	100nF/275V_{AC}	Box Capacitor	**IC**		
C103	33μF/400V	Electrolytic Capacitor	IC101	FSQ0365RN	FPS™
C104	10nF/630V	Film Capacitor	IC201	KA431 (TL431)	Voltage reference
C105	47nF/50V	Mono Capacitor	IC202	FOD817A	Opto-coupler
C106	100nF/50V	SMD (1206)	**Fuse**		
C107	22μF/50V	Electrolytic Capacitor	Fuse	2A/250V	
C110	33pF/50V	Ceramic Capacitor	**NTC**		
C201	470μF/35V	Electrolytic Capacitor	RT101	5D-9	
C202	470μF/35V	Electrolytic Capacitor	**Bridge Diode**		
C203	470μF/35V	Electrolytic Capacitor	BD101	2KBP06M2N257	Bridge Diode
C204	470μF/35V	Electrolytic Capacitor	**Line Filter**		
C205	1000μF/10V	Electrolytic Capacitor	LF101	40mH	
C206	1000μF/10V	Electrolytic Capacitor	**Transformer**		
C207	1000μF/10V	Electrolytic Capacitor	T101		
C208	1000μF/10V	Electrolytic Capacitor	**Varistor**		
C209	100nF /50V	Ceramic Capacitor	TNR	10D471K	

Typical Application Circuit of FSQ311

Application	FPS Device	Input Voltage Range	Rated Output Power	Output Voltage (Max. Current)
DVD Player Power Supply	FSQ311	85-265V_{AC}	8W	5.1V (0.9A) 3.3V (0.9A) 12V (0.03A) 16V (0.03A)

Features

- High efficiency (>70% at universal input)
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Reduce EMI noise through Valley Switching operation
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C107 of 47nF. If faster/slower triggering of OLP is required, C107 can be changed to a smaller/larger value (eg. 100nF for 60ms).
- The input voltage of V_{sync} must be higher than -0.3V. By proper voltage sharing by R106 & R107 resistors, the input voltage can be adjusted.
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improved surge immunity.

1. Schematic

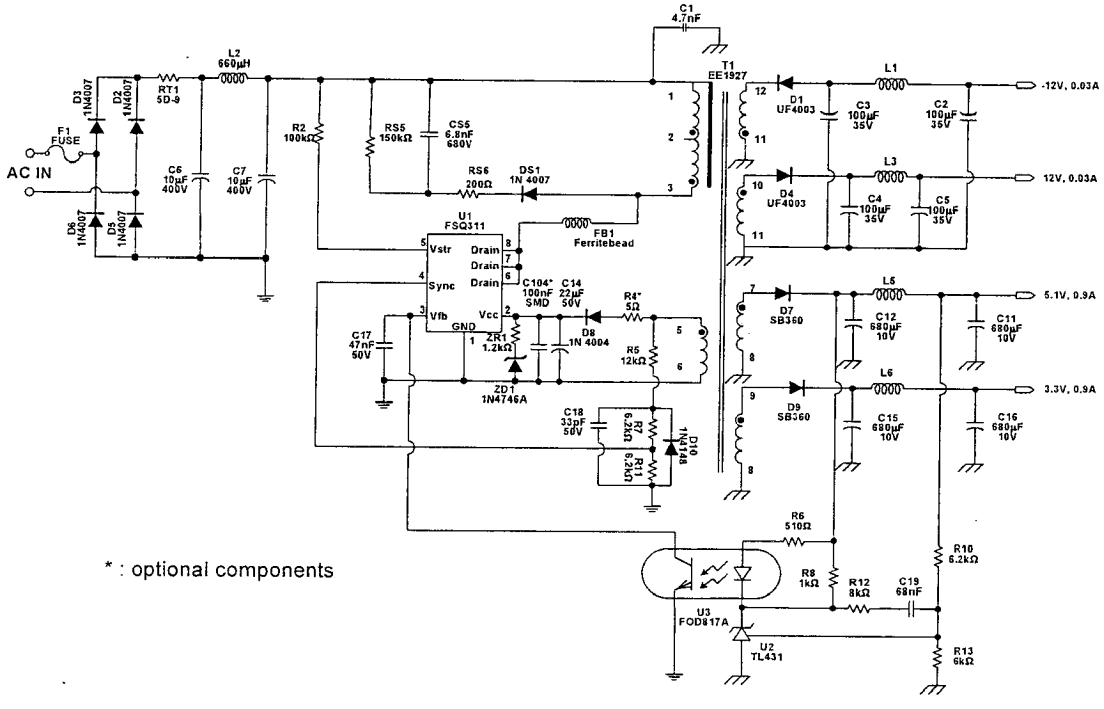


Figure 31. Demo Circuit of FSQ311

2. Transformer

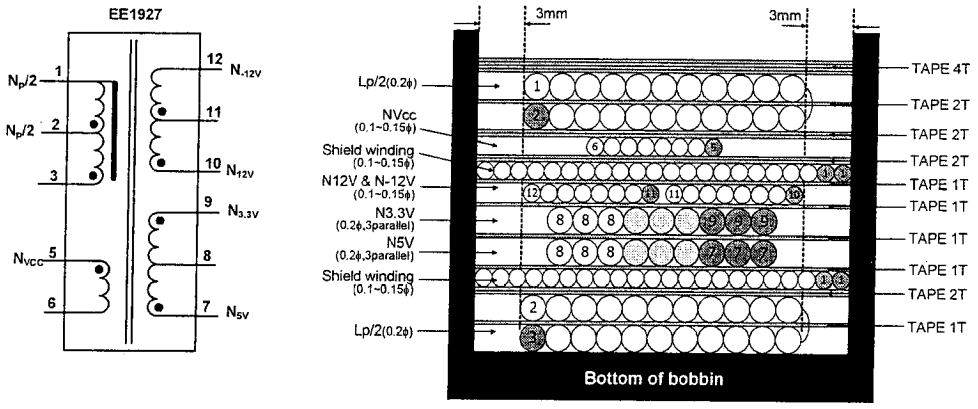


Figure 32. Transformer Schematic Diagram of FSQ311

3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.2^{\phi} \times 1$	111	Solenoid Winding, 2 Layers
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
Shield	1 → open	$0.1^{\phi} \times 2$		Shield winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
N_{5V}	7 → 8	$0.2^{\phi} \times 3$	15	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
$N_{3.3V}$	9 → 8	$0.2^{\phi} \times 3$	10	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
N_{12V}	10 → 11	$0.1^{\phi} \times 1$	30	Solenoid Winding
N_{-12V}	11 → 12	$0.1^{\phi} \times 3$	33	Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 1 Layer				
Shield	1 → open	$0.1^{\phi} \times 2$		Shield winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{VCCV}	5 → 6	$0.1^{\phi} \times 1$	36	Center Solenoid Winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	$0.2^{\phi} \times 1$	111	Solenoid Winding, 2 Layers
Insulation: Polyester Tape t = 0.025mm, 4 Layers				

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	2.1mH ± 10%	66kHz, 1V
Leakage	1 - 3	100μH Max.	Short all other pins

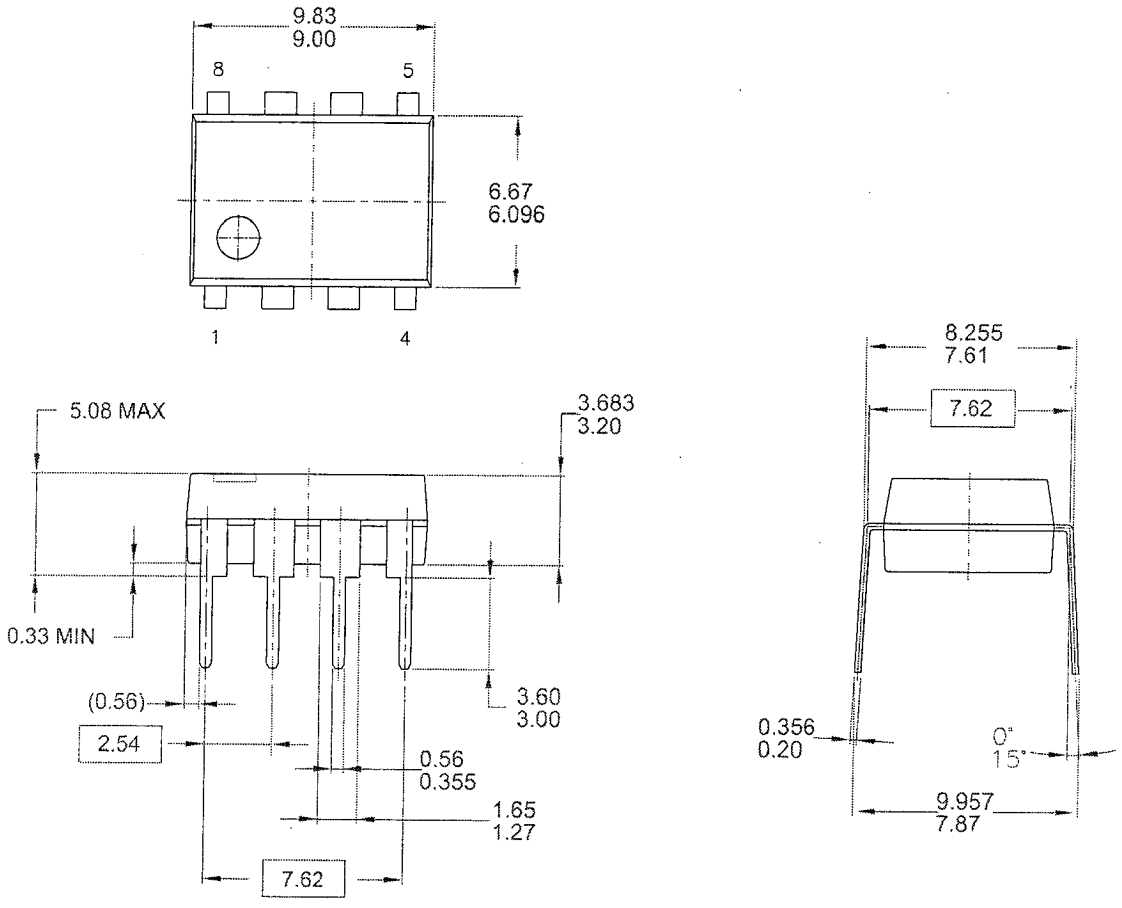
5. Core & Bobbin

- Core: EE1927 ($Ae=23.4mm^2$)
- Bobbin: EE1927

6. Demo Board Part List

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R2	100kΩ	1/4W	L2	660μH	
ZR1	1.2kΩ	1/4W	L1	4.7μH	
R4	5Ω	1/2W	L3	4.7μH	
R5	12kΩ	1/4W	L5	4.7μH	
R7	6.2kΩ	1/4W	L6	4.7μH	
R11	6.2kΩ	1/4W	**Diode**		
RS5	150kΩ	2W	D2,3,4,5	IN4007	
RS6	200Ω	1W	D8	IN4004	
R6	510Ω	1/4W	D10	1N4148	
R8	1kΩ	1/4W	ZD1	1N4746A	
R12	8kΩ	1/4W	DS1	1N4007	
R10	6.2kΩ	1/4W, 1%	D1	UF4003	
R13	6kΩ	1/4W, 1%	D4	UF4003	
Capacitor			D7	SB360	
C6	10μF/400V	Electrolytic	D9	SB360	
C7	10μF/400V	Electrolytic	**IC**		
C17	47nF/50V	Ceramic	U1	FSQ311	FPS™
C104	100nF/50V	SMD(1206)	U2	KA431 (TL431)	Voltage reference
C14	22μF/50V	Electrolytic	U3	FOD817A	Opto-coupler
C18	33pF/50V	Ceramic	**Fuse**		
CS5	6.8nF/680V	Film	Fuse	2A/250V	
C2	100μF/35V	Electrolytic	**NTC**		
C3	100μF/35V	Electrolytic	RT1	5D-9	
C4	100μF/35V	Electrolytic	**Transformer**		
C5	100μF/35V	Electrolytic	T1	EE1927	Bridge Diode
C11	680μF/10V	Electrolytic	**Ferrite bead**		
C12	680μF/10V	Electrolytic	FB1		
C15	680μF/10V	Electrolytic			
C16	680μF/10V	Electrolytic			
C19	68nμF/50V	Ceramic			
C1	4.7nF/375V_{AC}	Ceramic			

Package Dimensions



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D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 33. 8-Lead, Dual In-Line Package(DIP)

Package Dimensions (Continued)

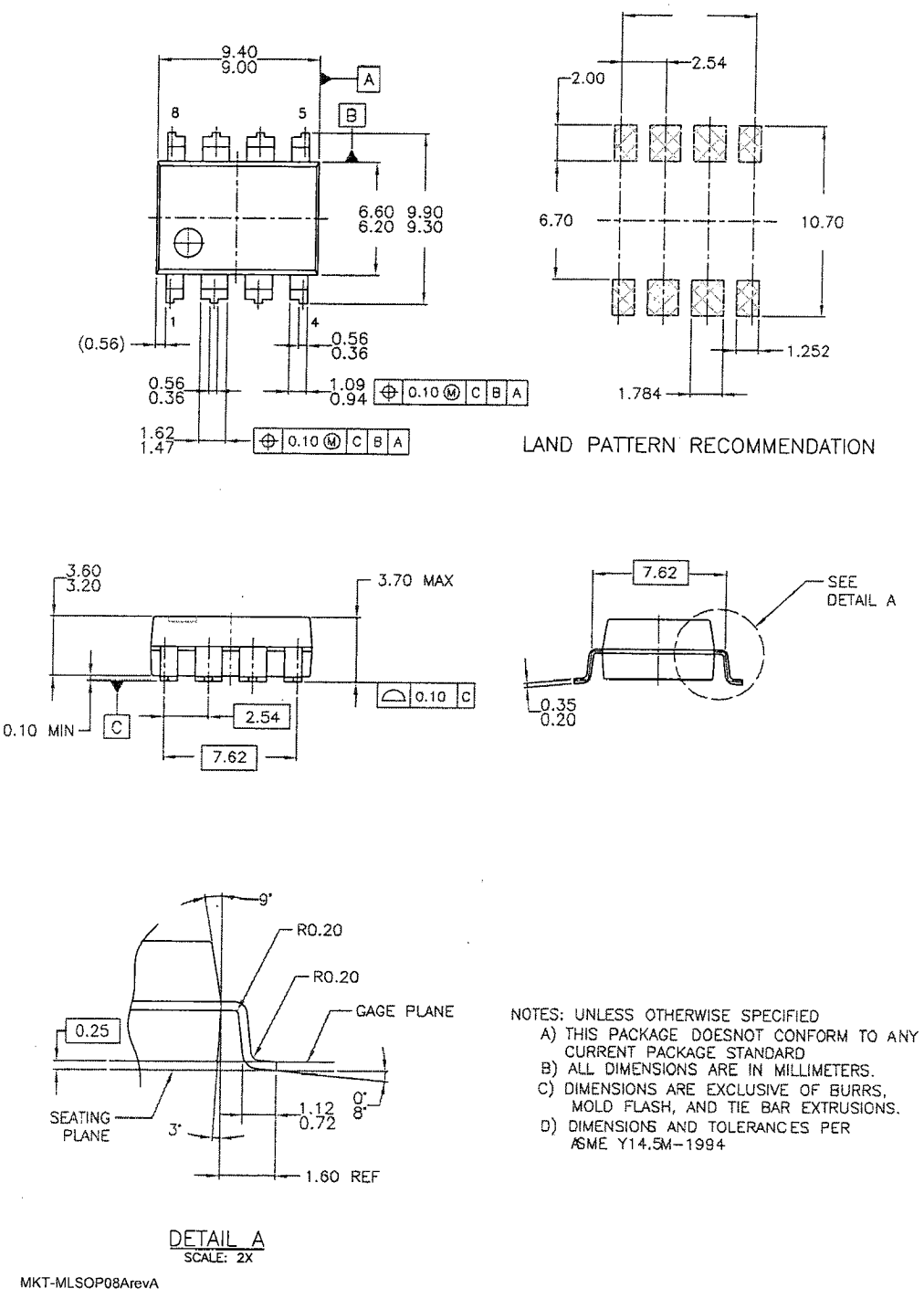

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Figure 34. 8-Lead, LSOP Package

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I31

EXHIBIT 4

FAIRCHILD SEMICONDUCTOR®

May 2007

FSQ510, FSQ510H
Green Mode Fairchild Power Switch (FPS™) for Valley Switching Converter – *Low EMI and High Efficiency*

Features

- Uses an LDMOS Integrated Power Switch
- Optimized for Valley Switching Converter (VSC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High Efficiency through Minimum Drain Voltage Switching
- Extended Valley Switching for Wide Load Ranges
- Small Frequency Variation for Wide Load Ranges
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Protection Functions: Overload Protection (OLP), Internal Thermal Shutdown (TSD) with Hysteresis
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage SenseFET (700V)
- Built-in Soft Start (5ms)

Applications

- Cell Phone Chargers
- Auxiliary Power Supplies for PC and White Goods

Description

A Valley Switching Converter (VSC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ510(H) is an integrated Valley Switching Pulse Width Modulation (VS-PWM) controller and SenseFET specifically designed for off-line Switch Mode Power Supplies (SMPS) for valley switching with minimal external components. The VS-PWM controller includes an integrated oscillator, Under-Voltage Lockout (UVLO), Leading Edge Blanking (LEB), optimized gate driver, internal soft start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry.

Compared with discrete MOSFET and PWM controller solutions, the FSQ510(H) can reduce total cost and component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a platform well suited for cost-effective designs of a valley switching flyback converters.

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Current Limit	$R_{DS(ON)}$ (MAX)	Output Power Table [1]				Replaces Devices
						230VAC ± 15%[2]		85-265VAC		
						Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]	
FSQ510	7-DIP	Yes	-40°C to +85°C	320mA	32Ω	5.5W	9W	4W	6W	FSD210B
FSQ510H	8-DIP	Yes	-40°C to +85°C	320mA	32Ω	5.5W	9W	4W	6W	FSD210DH

Notes:
1. The junction temperature can limit the maximum output power.
2. 230VAC or 100/115VAC with voltage doubler.
3. Typical continuous power with a Fairchild charger demo board described in this datasheet in a non-ventilated enclosed adapter housing measured at 50°C ambient temperature.
4. Maximum practical continuous power for auxiliary power supplies in an open-frame design at 50°C ambient temperature.

Application Circuit

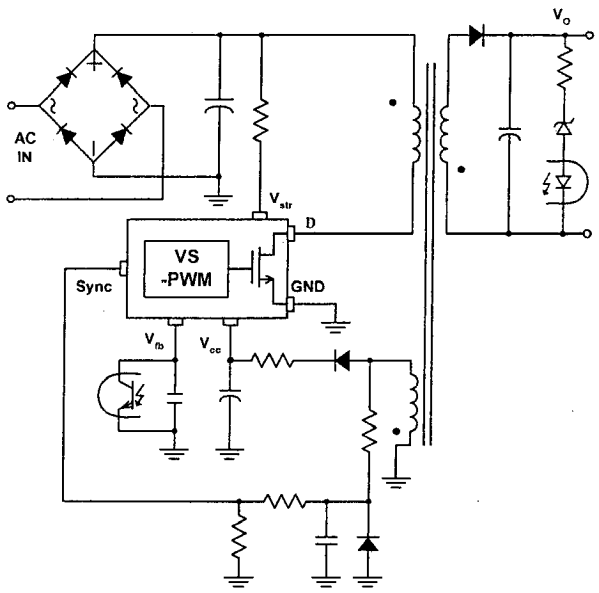


Figure 1. Typical Application Circuit

Internal Block Diagram

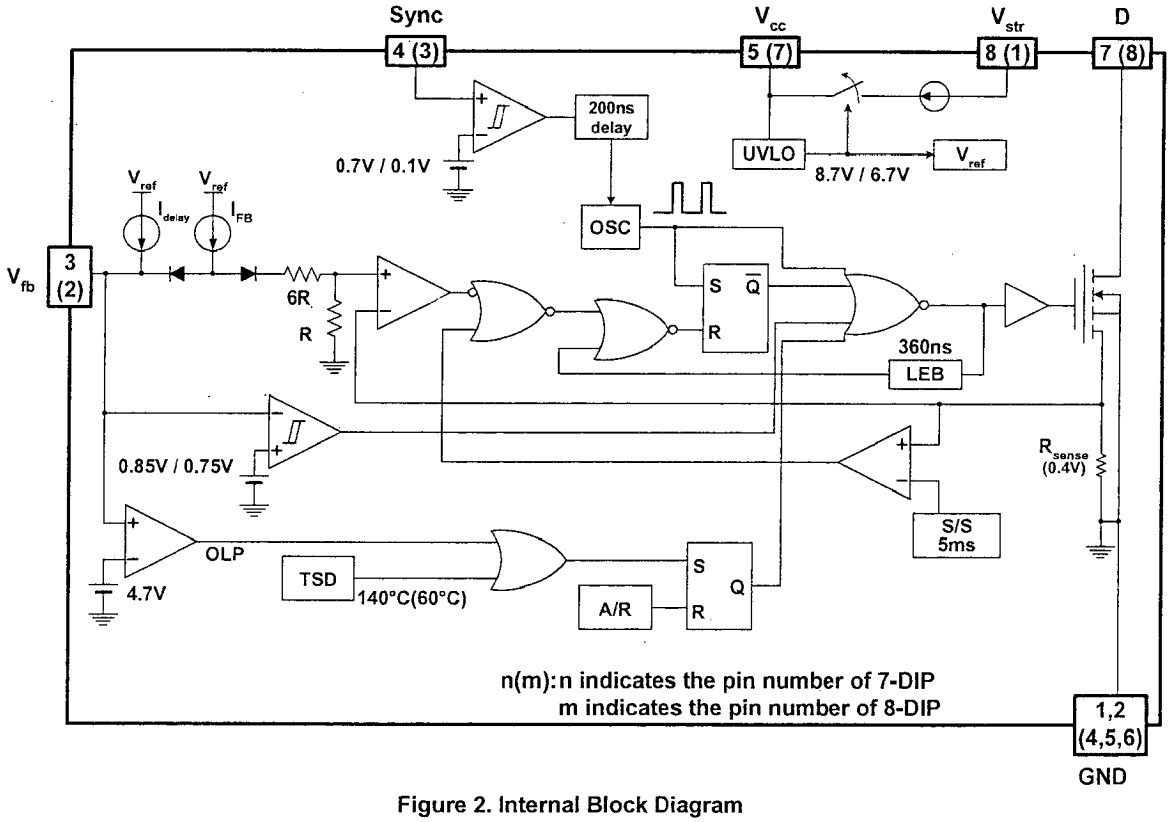


Figure 2. Internal Block Diagram

Pin Assignments

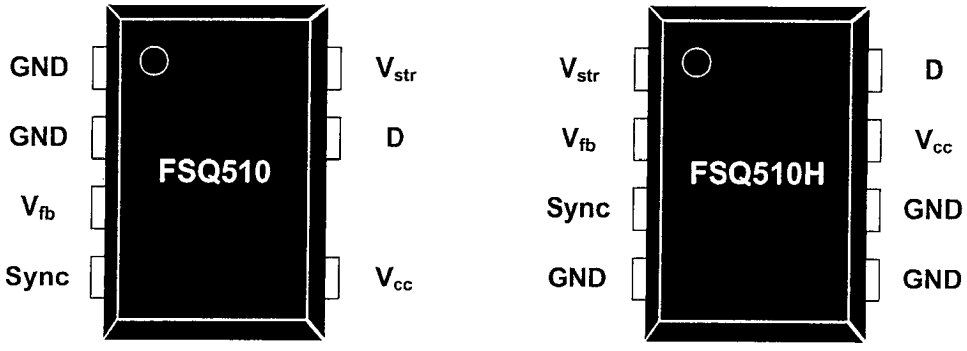


Figure 3. Package diagrams for FSQ510 and FSQ510H

Pin Definitions

Pin #	Name	Description
1,2[5] (4,5,6)[6]	GND	This pin is the control ground and the SenseFET source.
3 (2)	V_{fb}	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 4.7V, the overload protection triggers, which shuts down the FPS.
4 (3)	Sync	This pin is internally connected to the sync-detect comparator for valley switching. In normal valley switching operation, the threshold of the sync comparator is 0.7V/0.1V.
5 (7)	V_{CC}	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.
7 (8)	D	High-voltage power SenseFET drain connection.
8 (1)	V_{str}	This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 8.7V, the internal current source is disabled.

Notes:

5. Pin numbers for 7-DIP.
6. Pin numbers for 8-DIP are in parenthesis.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{STR}	V_{str} Pin Voltage			500	V
V_{DS}	Drain Pin Voltage			700	V
V_{CC}	Supply Voltage			20	V
V_{fb}	Feedback Voltage Range		-0.3	6.5	V
V_{Sync}	Sync Pin Voltage		-0.3	6.5	V
P_D	Total Power Dissipation	7-DIP		1.38	W
		8-DIP		1.47	W
T_J	Operating Junction Temperature		-40	Internally Limited	°C
T_A	Operating Ambient Temperature		-40	+85	°C
T_{STG}	Storage Temperature		-55	+150	°C

Thermal Impedance

T_A = 25°C, unless otherwise specified. All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	7-DIP	8-DIP	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance[7]	90	85	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance[8]	13	13	°C/W

Notes:

7. Free-standing with no heatsink; without copper clad. Measurement condition – just before junction temperature T_J enters into TSD.
8. Measured on the DRAIN pin close to plastic interface.

Electrical Characteristics

T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC} = 0V, I_D = 100μA	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = 700V			150	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	T_J = 25°C, I_D = 180mA		28	32	Ω
		T_J = 100°C, I_D = 180mA		42	48	Ω
C_{ISS}	Input Capacitance[9]	V_{GS} = 11V		96		pF
C_{OSS}	Output Capacitance[9]	V_{DS} = 40V		28		pF
t_r	Rise Time[9]	V_{DS} = 350V, I_D = 25mA		100		ns
t_f	Fall Time[9]	V_{DS} = 350V, I_D = 25mA		50		ns
Control Section						
f_S	Initial Switching Frequency	V_{CC} = 11V, V_{FB} = 0.5V, V_{sync} = 0V	87.7	94.3	100.0	kHz
Δf_S	Switching Frequency Variation[9]	- 25°C < T_J < 125°C		±5	±8	%
I_{FB}	Feedback Source Current	V_{CC} = 11V, V_{FB} = 0V	200	225	250	μA
t_B	Switching Blanking Time	V_{CC} = 11V, V_{FB} = 1V, V_{sync} frequency sweep	7.2	7.6	8.2	μs
t_W	Valley Detection Window Time[9]			3.0		μs
D_{MAX}	Maximum Duty Ratio	V_{CC} = 11V, V_{FB} = 3V	54	60	66	%
D_{MIN}	Minimum Duty Ratio	V_{CC} = 11V, V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = 0V, V_{CC} sweep	8.0	8.7	9.4	V
V_{STOP}		After Turn-on, V_{FB} = 0V	6.0	6.7	7.4	V
$t_{S/S}$	Internal Soft-Start Time	V_{STR} = 40V, V_{CC} sweep	3	5	7	ms
Burst-Mode Section						
V_{BURH}	Burst-Mode Voltage	V_{CC} = 11V, V_{FB} sweep	0.75	0.85	0.95	V
V_{BURL}			0.65	0.75	0.85	V
Hys.				100		mV
Protection Section						
I_{LIM}	Peak Current Limit	di/dt = 90mA/μs	280	320	360	mA
V_{SD}	Shutdown Feedback Voltage	V_{DS} = 40V, V_{CC} = 11V, V_{FB} sweep	4.2	4.7	5.2	V
I_{DELAY}	Shutdown Delay Current	V_{CC} = 11V, V_{FB} = 5V	4	5	6	μA
t_{LEB}	Leading Edge Blanking Time[9]			360		ns
T_{SD}	Thermal Shutdown Temperature[9]		130	140	150	°C
Hys.				60		°C
Sync Section						
V_{SH}	Sync Threshold Voltage	V_{CC} = 11V, V_{FB} = 1V	0.55	0.70	0.85	V
V_{SL}		V_{CC} = 11V, V_{FB} = 1V	0.05	0.10	0.15	V
t_{Sync}	Sync Delay Time		180	200	220	ns
Total Device Section						
I_{OP}	Operating Supply Current (Control Part Only)	V_{CC} = 11V, V_{FB} = 5.5V		0.8	1.0	mA
I_{CH}	Start-up Charging Current	V_{CC} = V_{FB} = 0V, V_{STR} = 40V		1.0	1.2	mA
V_{STR}	Supply Voltage	V_{CC} = V_{FB} = 0V, V_{STR} sweep		27		V

Notes:

9. These parameters, although guaranteed, are not 100% tested in production.

Comparison Between FSD210B and FSQ510

Function	FSD210B	FSQ510	Advantages of FSQ510
Control Mode	Voltage Mode	Current Mode	Fast response Easy-to-design control loop
Operation Method	Constant Frequency PWM	Valley Switching Operation	Turn-on at minimum drain voltage High efficiency and low EMI
EMI Reduction Method	Frequency Modulation	Valley Switching	Frequency variation depending on the ripple of DC link voltage High efficiency and low EMI
Soft Start	3ms (Built-in)	5ms (Built-in)	Longer soft-start time
Protection	TSD	TSD with hysteresis	Enhanced thermal shutdown protection
Power Balance	Long T_{CLD}	Short T_{CLD}	The difference of input power between low and high input voltage is quite small.
Power Ratings	Less than 5W under open frame condition at the universal line input	More than 6W under open frame condition at the universal line input	More output power ratings available due to the valley switching.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A = 25°C.

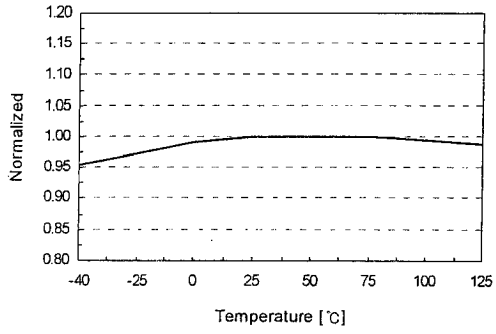


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

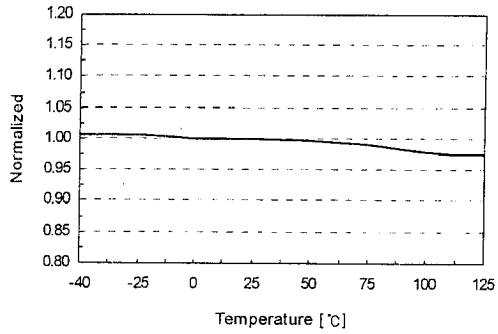


Figure 5. Peak Current Limit (I_{LIM}) vs. T_A

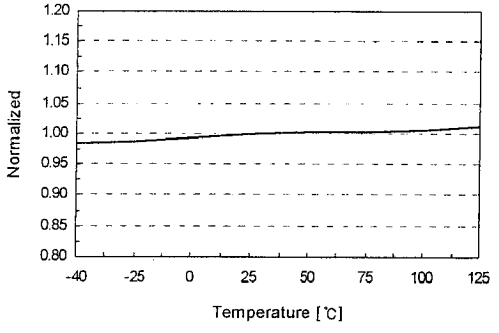


Figure 6. Start Threshold Voltage (V_{START}) vs. T_A

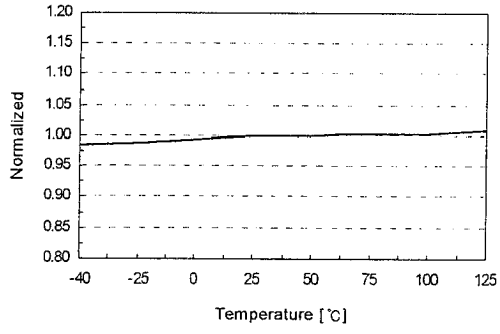


Figure 7. Stop Threshold Voltage (V_{STOP}) vs. T_A

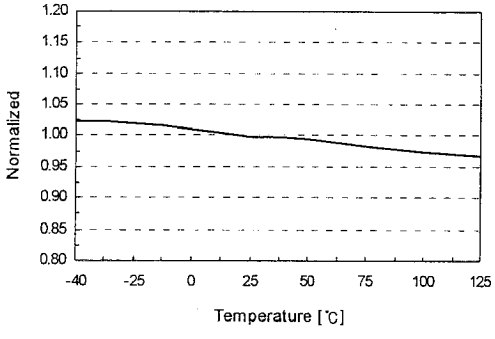


Figure 8. Shutdown Feedback Voltage (V_{SD}) vs. T_A

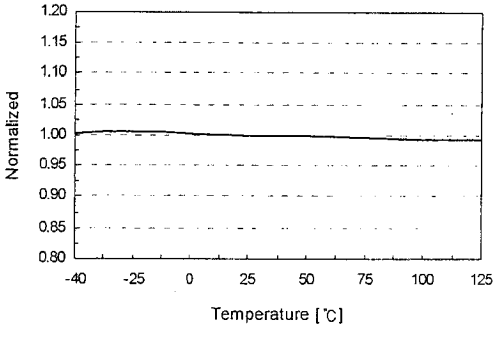


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

Typical Performance Characteristics (Continued)

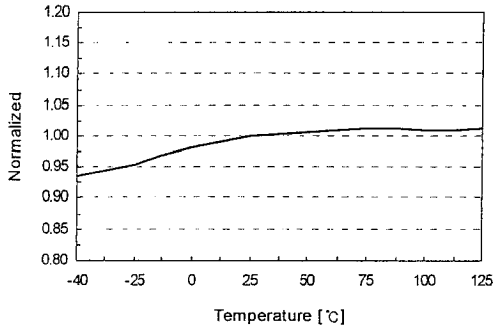


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

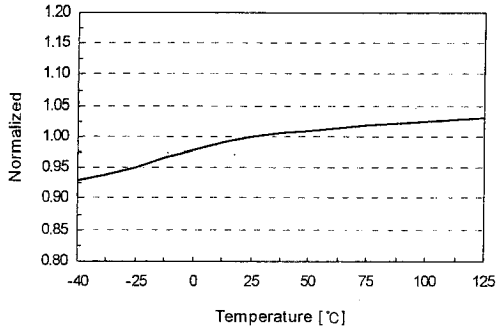


Figure 11. Shutdown Delay Current (I_{DELAY}) vs. T_A

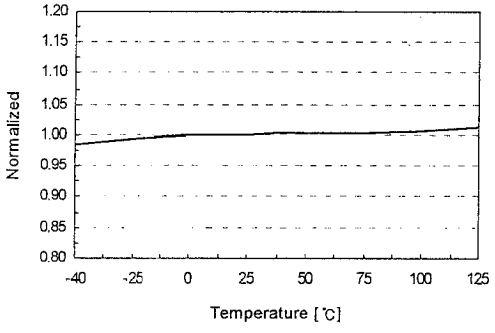


Figure 12. Operating Supply Current (I_{OP}) vs. T_A

Functional Description

1. Start-up: At start-up, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 13. When V_{CC} reaches 8.7V, the FPS begins switching and the internal high-voltage current source is disabled. The FPS continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 6.7V.

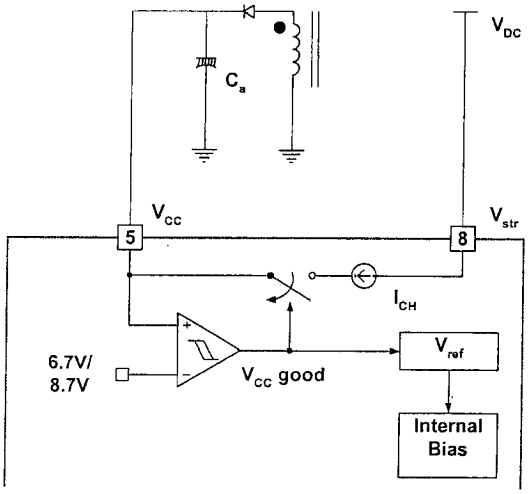


Figure 13. Start-up Block

2. Feedback Control: This device employs current mode control, as shown in Figure 14. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the drain current. This event typically occurs when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{fb}*), as shown in Figure 14. Assuming that the 225μA current source flows only through the internal resistor (6R + R = 12.6 kΩ), the cathode voltage of diode D2 is about 2.8V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.8V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode VS-PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the VS-PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

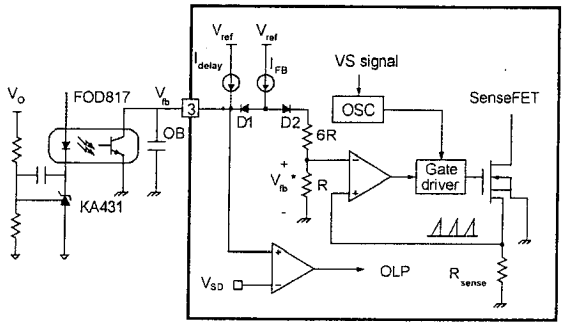


Figure 14. Valley Switching Pulse Width Modulation (VS-PWM) Circuit

3. Synchronization: The FSQ510(H) employs a valley switching technique to minimize the switching noise and loss. The basic waveforms of the valley switching converter are shown in Figure 15. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 15. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 15.

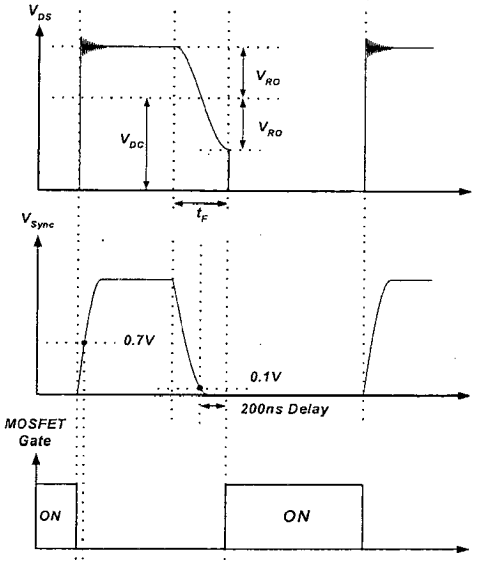


Figure 15. Valley Switching Waveforms

4. Protection Circuits: The FSQ510(H) has two self-protective functions: Overload Protection (OLP) and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 6.7V, the protection is reset and the start-up circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 8.7V, the FSQ510(H) resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

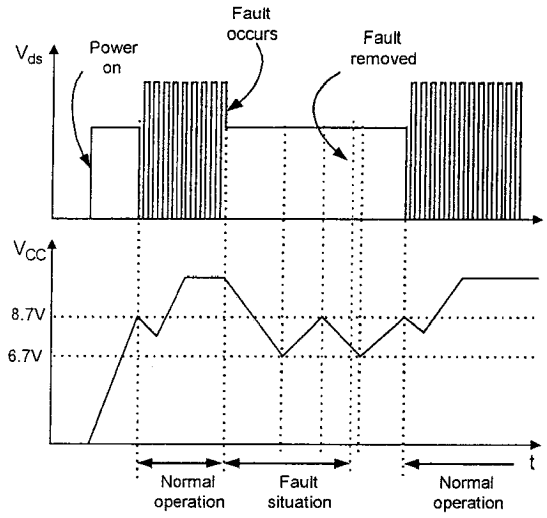


Figure 16. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_o) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.8V, D1 is blocked and the 5μA current source starts to charge C_B slowly up. In this condition, Vfb continues increasing until it reaches 4.7V, when the switching operation is terminated, as shown in Figure 17. The delay time for shutdown is the time required to charge C_B from 2.8V to 4.7V with 5μA. A 20 ~ 50ms delay time is typical for most applications. This protection is implemented in auto restart mode.

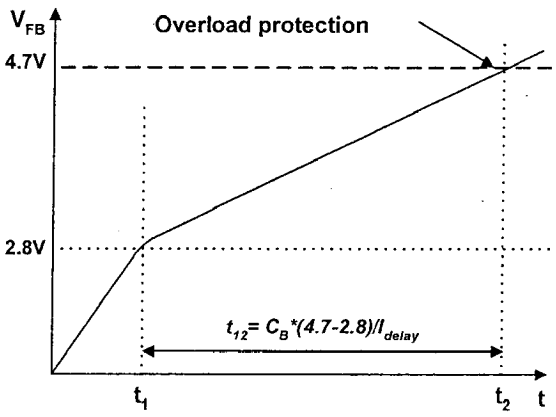


Figure 17. Overload Protection

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers. The FPS stops operation at that time. The FPS operates in auto-restart mode until the temperature decreases to ~80°C, then normal operation resumes.

5. Soft-Start: The FPS has an internal soft-start circuit that increases VS-PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts up. The typical soft-start time is 5ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This helps prevent transformer saturation and reduce stress on the secondary diode - during start-up.

6. Burst-Mode Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 18, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (850mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the SenseFET, thereby reducing switching loss in standby mode.

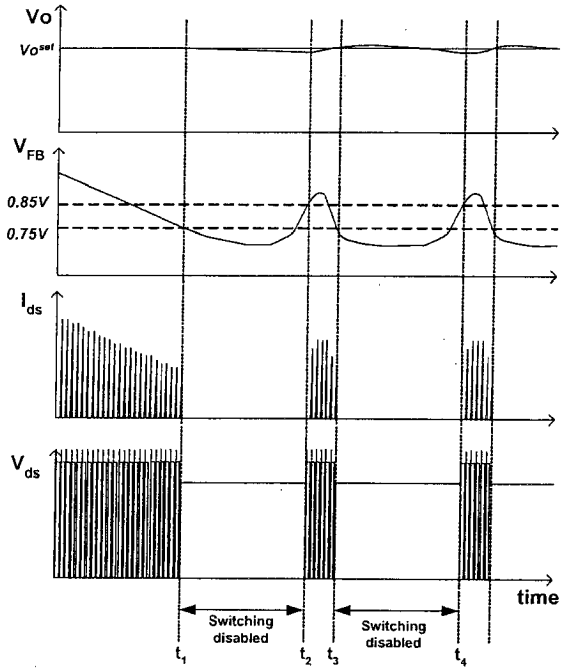


Figure 18. Burst-Mode Operation

7. Advanced Valley Switching Operation: To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in VS converters. Due to the Discontinuous Conduction Mode (DCM) operation, the feedback voltage is not changed, despite the DC link voltage ripple, if the load condition is not changed. Since the slope of the drain current is changed depending on the DC link voltage, the turn-on duration of MOSFET is variable with the DC link voltage ripple. The switching period is changed continuously with the DC link voltage ripple. Switching at the instant of the minimum drain voltage and the continuous change of the switching period reduces EMI. VS converters inherently scatter the EMI spectrum.

Typical products for VSC turn the MOSFET on when the first valley is detected. In this case, the range of the switching frequency is very wide as a result of the load variations. At a very light load, for example, the switching frequency can be as high as several hundred kHz. Some products for VSC, such as Fairchild's FSCQ-series, define the turn-on instant of SenseFET changing at the first valley into the second valley when the load condition decreases below its predetermined level. The range of switching frequency narrows somewhat. For details, consult an FSCQ-series datasheet, such as:
http://www.fairchildsemi.com/pf/FS/FSCQ1265RT.html

The range of the switching frequency can be limited tightly in FSQ-series. Because a kind of blanking time (t_B) is adopted, as shown in Figure 19, the switching frequency has minimum and maximum values.

Once the SenseFET is enabled, the next start is prohibited during the blanking time (t_B). After the blanking time, the controller finds the first valley within the duration of the valley-detection window time (t_W) (Case A, B, and C). If no valley is found in t_W, the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, FSQ510 and FSQ510H have a minimum switching frequency of 94.3kHz and maximum switching frequency of 132kHz typically, as shown in Figure 20.

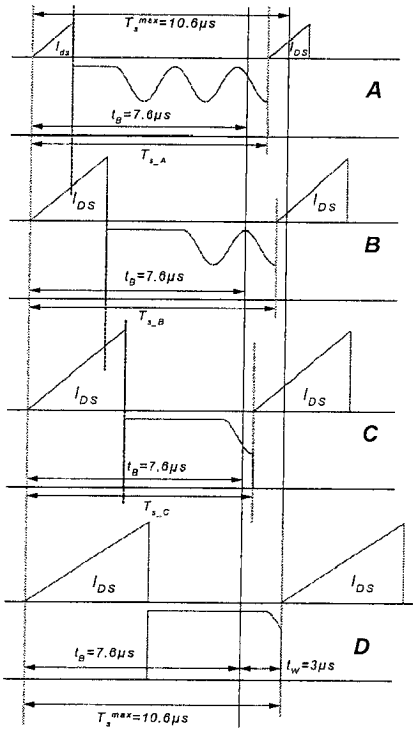


Figure 19. Advanced VS Operation

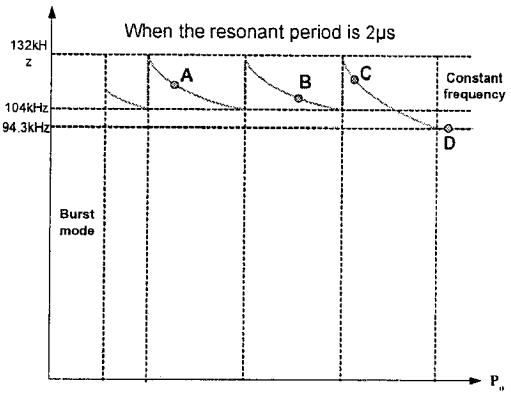
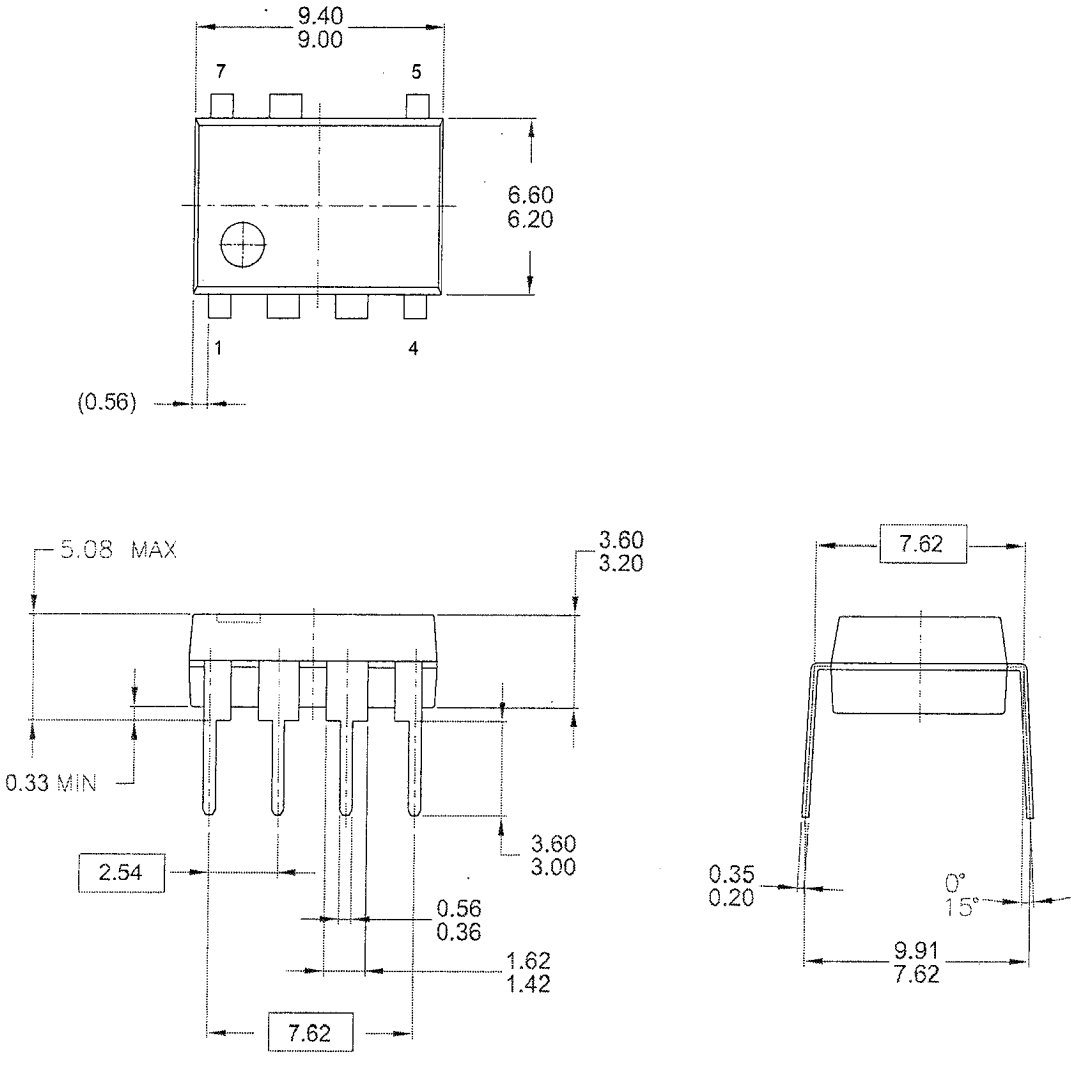


Figure 20. Switching Frequency Range of the Advanced Valley Switching

Package Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE COMPLIES TO JEDEC MS-001, VARIATION BA, EXCEPT FOR TERMINAL COUNT (7 RATHER THAN 8)

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

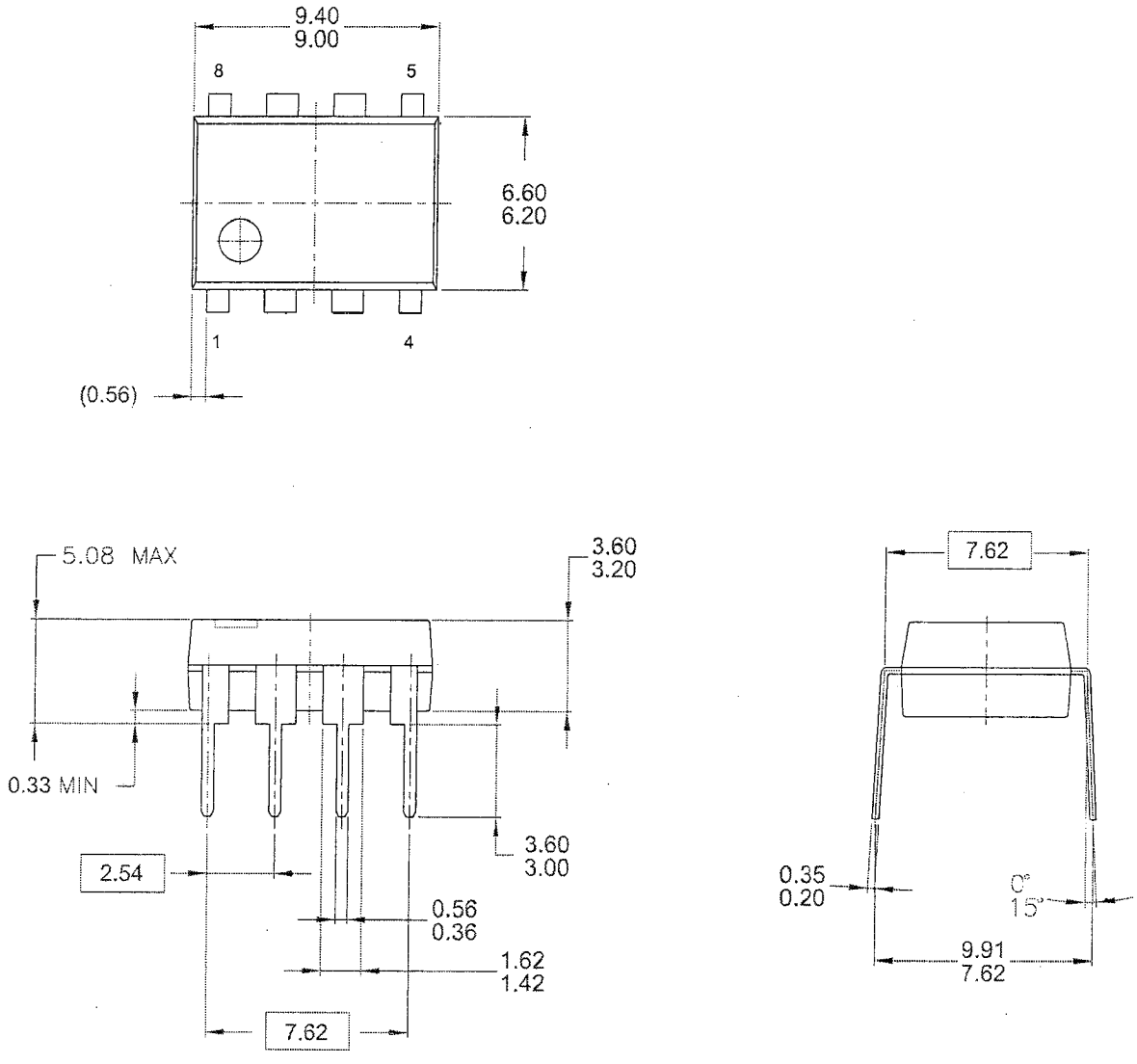
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-NA07BrevA

Figure 21. 7-Pin Dual Inline Package (DIP)

Package Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED:

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5 M-1994.

MKT-N08FrevA

Figure 22. 8-Pin Dual Inline Package (DIP)

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I28

EXHIBIT 5

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Ex Parte Reexamination Filing Data - September 30, 2007

1. Total requests filed since start of ex parte reexam on 07/01/81 . . . . . 8895[1]

a. By patent owner	3472	39%
b. By other member of public	5258	59%
c. By order of Commissioner	165	2%

2. Number of filings by discipline

a. Chemical Operation	2671	30%
b. Electrical Operation	2958	33%
c. Mechanical Operation	3266	37%

3. Annual Ex Parte Reexam Filings

Fiscal Yr.	No.	Fiscal Yr.	No.	Fiscal Yr.	No.	Fiscal Yr.	No.
1981	78 (3 mos.)	1989	243	1997	376	2005	524
1982	187	1990	297	1998	350	2006	511
1983	186	1991	307	1999	385	2007	643
1984	189	1992	392	2000	318		
1985	230	1993	359	2001	296		
1986	232	1994	379	2002	272		
1987	240	1995	392	2003	392		
1988	268	1996	418	2004	441		

4. Number known to be in litigation 2303 26%

5. Determinations on requests 8557

a. No. granted . . . . . 7845 . . . . . 92%

(1) By examiner	7732
(2) By Director (on petition)	113

b. No. denied . . . . . 712 . . . . . 8%

(1) By examiner	677
(2) Order vacated	35

[1]Of the requests received in FY 2007, 23 requests have not yet been accorded a filing date, and preprocessing of 36 requests was terminated for failure to comply with the requirements of 37 CFR 1.510. See Clarification of Filing Date Requirements for *Ex Parte* and *Inter Partes* Reexamination Proceedings, Final Rule, 71 Fed. Reg. 44219 (August 4, 2006).

6. Total examiner denials (includes denials reversed by Director) 790

a. Patent owner requester	439	56%
b. Third party requester	351	44%

7. Overall reexamination pendency (Filing date to certificate issue date)

a. Average pendency	23.7 (mos.)
b. Median pendency	18.4 (mos.)

8. Reexam certificate claim analysis:

	Owner Requester	3rd Party Requester	Comm'r Initiated	Overall
a. All claims confirmed	23%	29%	12%	26%
b. All claims cancelled	7%	12%	21%	10%
c. Claims changes	70%	59%	67%	64%

9. Total ex parte reexamination certificates issued (1981 - present) 5902

a. Certificates with all claims confirmed	1527	26%
b. Certificates with all claims canceled	613	10%
c. Certificates with claims changes	3762	64%

10. Reexam claim analysis - requester is patent owner or 3rd party; or Comm'r initiated.

a. Certificates - PATENT OWNER REQUESTER 2545

(1) All claims confirmed	581	23%
(2) All claims canceled	187	7%
(3) Claim changes	1777	70%

b. Certificates - 3rd PARTY REQUESTER 3211

(1) All claims confirmed	928	29%
(2) All claims canceled	397	12%
(3) Claim changes	1886	59%

c. Certificates - COMM'R INITIATED REEXAM 146

(1) All claims confirmed	18	12%
(2) All claims canceled	30	21%
(3) Claim changes	98	67%